



3A 6000

V1.2

2024 07





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3A6000

3A6000







ESDA

KKK

終正有限公司
Loo Corporation Limited

3A6000



3A6000

33- 6

ZK



3A6000

36- 5; JV	3	0000000000000000 335
36- 62 JV	4	0000000000000000 335
36- 63 JV	4	0000000000000000 336



00

ZK

00000000 0002

00

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* * * * *

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* * * * *

3A6000



1

1.1

1

32

2

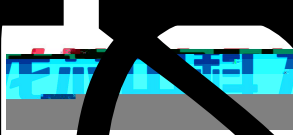
32

64

SoC

3

64



3A6000

S0 S1 S2 S3

Master/Slave

EMES SM/SS WM/VS NM/NS

X2

Master

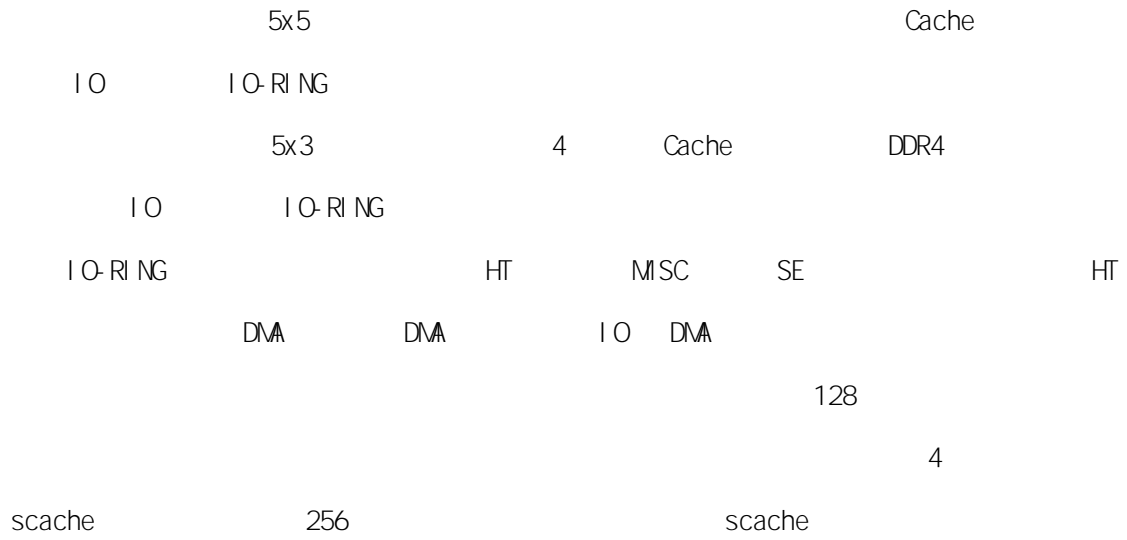
Cache

Slave

Slave

Xconf

X1 X2



2

2.1

3A6000

4 8

2.2

DO_TEST CHIP_CONFIG[9:0]

2- 1



```
DO_TEST      1' b1
              1' b0
              ]
```

CHIP_CONFIG[9:4]



3

3

48

4

16

44

3A6000

44

3.1

3A6000

4 8



4' h3	13: 12	4' hb	29: 28
4' h4	15: 14	4' hc	31: 30
4' h5	17: 16	4' hd	33: 32
4' h6	19: 18	4' he	35: 34
4' h7	21: 20	4' hf	37: 36

3A6000 44 MC
interleave IOCSR[0x400]

3- 3 44

addr[43:40] == 4' hc	, uncache	SE
addr[43:40] == 4' he	, uncache	HT
0x10000000-0x1fffffff, 0x3ff00000-0x3ff0ffff ()	, uncache	MISC
Master interleave 0	, uncache	MC0
Master interleave 1	, uncache	MC1
Scache interleave 0(sci_d_sel)	, cache	Scache0
Scache interleave 1(sci_d_sel)	, cache	Scache1
Scache interleave 2(sci_d_sel)	, cache	Scache2
Scache interleave 3(sci_d_sel)	, cache	Scache3

3.2

3A6000 IO-RING
Master 8
8 BASE MASK MMAP 64
BASE K MASK 1 MMAP
Slave MMAP[4] MMAP[5] MMAP[6]
MMAP[7]

3- 4 MMAP

[7]	[6]	[5]	[4]
	SCACHE/		

: (I N_ADDR & MASK) == BASE

3



SCACHE/ Slave 0 4 0
 SCACHE SCI D_SEL 4 SCACHE 4
 interleaved bit 2 MC
 OX1FE0_0000 ICCSR

3- 5

0x2000	CORE0_WN0_BASE	0x2100	CORE1_WN0_BASE
0x2008	CORE0_WN1_BASE	0x2108	CORE1_WN1_BASE
0x2010	CORE0_WN2_BASE	0x2110	CORE1_WN2_BASE
0x2018	CORE0_WN3_BASE	0x2118	CORE1_WN3_BASE
0x2020	CORE0_WN4_BASE	0x2120	CORE1_WN4_BASE
0x2028	CORE0_WN5_BASE	0x2128	CORE1_WN5_BASE
0x2030	CORE0_WN6_BASE	0x2130	CORE1_WN6_BASE
0x2038	CORE0_WN7_BASE	0x2138	CORE1_WN7_BASE
0x2040	CORE0_WN0_MASK		



0x2238	CORE2_W N7_BASE	0x2338	CORE3_W N7_BASE
0x2240	CORE2_W NO_MASK	0x2340	CORE3_W NO_MASK
0x2248	CORE2_W N1_MASK	0x2348	CORE3_W N1_MASK
0x2250	CORE2_W N2_MASK	0x2350	CORE3_W N2_MASK
0x2258	CORE2_W N3_MASK	0x2358	CORE3_W N3_MASK
0x2260	CORE2_W N4_MASK	0x2360	CORE3_W N4_MASK
0x2268	CORE2_W N5_MASK	0x2368	CORE3_W N5_MASK
0x2270	CORE2_W N6_MASK	0x2370	CORE3_W N6_MASK
0x2278	CORE2_W N7_MASK	0x2378	CORE3_W N7_MASK
0x2280	CORE2_W NO_MAP	0x2380	CORE3_W NO_MAP
0x2288	CORE2_W N1_MAP	0x2388	CORE3_W N1_MAP
0x2290	CORE2_W N2_MAP	0x2390	CORE3_W N2_MAP
0x2298	CORE2_W N3_MAP	0x2398	CORE3_W N3_MAP
0x22a0	CORE2_W N4_MAP	0x23a0	CORE3_W N4_MAP
0x22a8	CORE2_W N5_MAP	0x23a8	CORE3_W N5_MAP
0x22b0	CORE2_W N6_MAP	0x23b0	CORE3_W N6_MAP
0x22b8	CORE2_W N7_MAP	0x23b8	CORE3_W N7_MAP
0x2400	SCACHE0_W NO_BASE	0x2500	SCACHE1_W NO_BASE
0x2408	SCACHE0_W N1_BASE	0x2508	SCACHE1_W N1_BASE
0x2410	SCACHE0_W N2_BASE	0x2510	SCACHE1_W N2_BASE
0x2418	SCACHE0_W N3_BASE	0x2518	SCACHE1_W N3_BASE
0x2420	SCACHE0_W N4_BASE	0x2520	SCACHE1_W N4_BASE
0x2428	SCACHE0_W N5_BASE	0x2528	SCACHE1_W N5_BASE
0x2430	SCACHE0_W N6_BASE	0x2530	SCACHE1_W N6_BASE
0x2438	SCACHE0_W N7_BASE	0x2538	SCACHE1_W N7_BASE
0x2440	SCACHE0_W NO_MASK	0x2540	SCACHE1_W NO_MASK
0x2448	SCACHE0_W N1_MASK	0x2548	SCACHE1_W N1_MASK
0x2450	SCACHE0_W N2_MASK	0x2550	SCACHE1_W N2_MASK
0x2458	SCACHE0_W N3_MASK	0x2558	SCACHE1_W N3_MASK
0x2460	SCACHE0_W N4_MASK	0x2560	SCACHE1_W N4_MASK
0x2468	SCACHE0_W N5_MASK	0x2568	SCACHE1_W N5_MASK
0x2470	SCACHE0_W N6_MASK	0x2570	SCACHE1_W N6_MASK
0x2478	SCACHE0_W N7_MASK	0x2578	SCACHE1_W N7_MASK
0x2480	SCACHE0_W NO_MAP	0x2580	SCACHE1_W NO_MAP
0x2488	SCACHE0_W N1_MAP	0x2588	SCACHE1_W N1_MAP
0x2490	SCACHE0_W N2_MAP	0x2590	SCACHE1_W N2_MAP
0x2498	SCACHE0_W N3_MAP	0x2598	SCACHE1_W N3_MAP
0x24a0	SCACHE0_W N4_MAP	0x25a0	SCACHE1_W N4_MAP
0x24a8	SCACHE0_W N5_MAP	0x25a8	SCACHE1_W N5_MAP
0x24b0	SCACHE0_W N6_MAP	0x25b0	SCACHE1_W N6_MAP

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-	-	0x2970	IO_L2X_WN6_MASK
-	-	0x2978	IO_L2X_WN7_MASK
-	-	0x2980	IO_L2X_WN0_MMAP
-	-	0x2988	IO_L2X_WN1_MMAP
-	-	0x2990	IO_L2X_WN2_MMAP
-	-		



3- 8 MMAP

[7]	[6]	[5]	[4]
	DDR interleave_bit CCSR[0x0400]	0 "	
		10	

Cache

SCache

Cache

Cache

: (IN_ADDR & MASK) == BASE

: OUT_ADDR = (IN_ADDR & ~MASK) | {MMAP[63:10], 10'h0}

CPU 0x00000000 - 0x0fffffff

256M

DDR 0x00000000 - 0x0fffffff

0x10000000-0x17fffffff

PCI_MEM

0x18000000-0x19fffffff

PCI_IO

0x1a000000-0x1affffff

PCI

Type0

0x1b000000-0x1bffffff

PCI

Type1

0x40000000-0x7fffffff

PCI_MEM

CPU

8

CPU



7	DVFS_v1	R	1' b1	1	v1
8	Tsensor	R	1' b1	1	
9		R	1' b1		
10		R	1' b1		
11	Guest Mode	R	1' b0	KVM	
12	Freq_scale_16	R	1' b0	1	16
13	Int_Remap	R	1' b1	1	
14	SE_enabled	R	1' b0	1	SE

4.3 0x0010

0x0010

4- 4

63: 0	Vendor	R	0x6e6f7367_6e6f6f4c	" Loongson"
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4.4 0x0020

0x0020

4- 5

63: 0	ID	R	0x00003030_30364133	" 3A6000"
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4.5 0x0180

0x0180

4- 6

0		RW	1' b0	
1		RW	1' b0	
3: 2		RW	2' b0	
4	M0_di_sabl_e_conf space	RW	1' b0	M0 DDR
5	M0_deful t_conf space	RW	1' b1	
6		RW	1' b1	
7	M0_resetn	RW	1' b1	M0
8	M0_cl ken	RW	1' b1	M0
9	M1_di_sabl_e_conf space	RW	1' b0	M1 W



10	MC1_deful t_conf space	RW	1' b1	
11		RW	1' b1	
12	MC1_res etn	RW	1' b1	MC1
13	MC1_cl ken	RW	1' b1	MC1
26: 24	HT_freq_scal e_ctrl	RW	3' b011	HT
27	HT_cl ken	RW	1' b1	HT
30: 28				
31				
42: 40	Nbde_freq_ ctrl	RW	3' b111	
43	-	RW	1' b1	
63: 56	Cpu_versi on	R	2' h3F	CPU

4.6

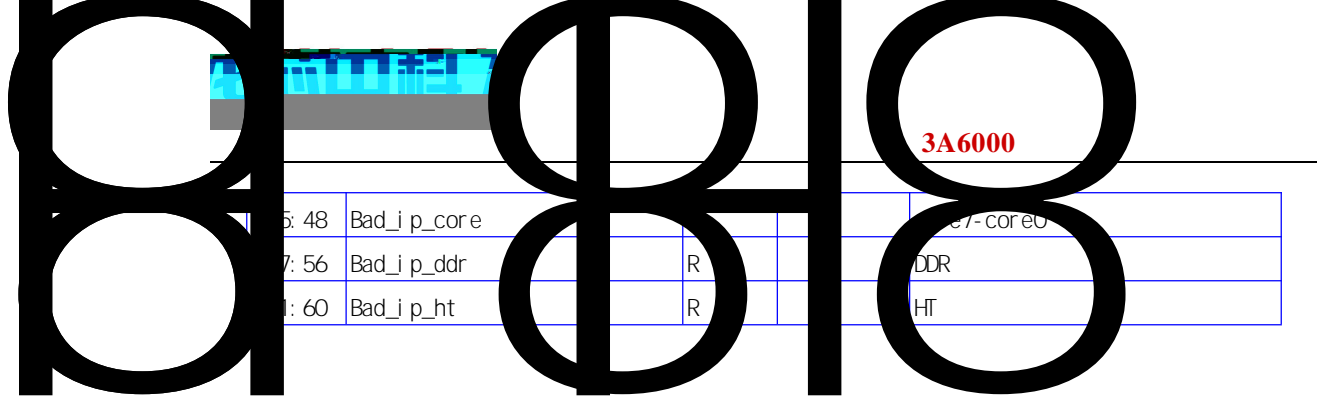
0x0188

0x0188

4- 7



15: 0				
19: 16	HT si deband	RW	4' b0	HT
23: 20	I 2C	RW	4' b0	I 2C
27: 24	UART	RW	4' b0	UART
31: 28	SPI	RW	4' b1	SPI
35: 32	GPI O	RW	4' b0	GPI O
39: 36	SE UART	RW	4' b0	SE UART
43: 40	SE SPI	RW	4' b0	SE SPI
47: 44	SE I 2C	RW	4' b0	SE I 2C
51: 48	É			I



4.8

8

V



1)

63: 63	L2_DIV_L	RW	L2
64: 64	L2_DIV_C	RW	L2 2 N
69: 67			
71: 71	L2_REFD	RW	3' b000
75: 73	L2_FBDLY	RW	3' b000
79: 76	L2_I_CPSEL	RW	4' b0111
83: 80	L2_FVCO_TUNE_ABS	RW	4' b0011
84	L2_SSC_SPRD	RW	0
85	L2_SSC_EN	RW	L2
95: 86	-	RW	
115: 96	L2_FRAC	RW	L2
119: 116			
122: 120	VDDA_LDO_CTRL	RW	
123	VDDA_LDO_BYPASS	RW	
126: 124	VDDD_LDO_CTRL	RW	
127: 124	VDDD_LDO_BYPASS	RW	
	-	RW	

PLL ouput = clk_r



				NODE	NODE_CLOCK_SEL	1
[23: 14]	MEM_PLL_DIV_LOOPC	RW	0x41	MEM_PLL		
[29: 24]	MEM_PLL_DIV_OUT	RW	0x0	MEM_PLL		
[30]	NODE_CLOCK_SEL	RW	0x0	0	MEM_PLL	MEM
[31]	-			1	NODE_CLOCK	L2_PLL
[34: 32]	VDDA_LDO_CTRL	RW				
[35]	VDDA_LDO_BYPASS	RW				
[38: 36]	VDDD_LDO_CTRL	RW				
[39]	VDDD_LDO_BYPASS	RW				
[40]						



3A6000

11	core2_en	RW	0x1	2	1
14:12	core3_freqctrl	RW	0x7	3	
15	core3_en	RW	0x1	3	

:

+1 /8



12		RW	0x0	
14	Scache_1MB	RW	0x0	Scache
19: 16		RW	0x0	
24		RW	0x0	
31: 30	mc_en	RW	0x3	MC
37: 32	i nterl eave_bi t	RW	0x0	
39	i nterl eave_en	RW	0x0	
43: 40	ht_control	R		Ht
47: 44		RW	0x0	
60: 56		RW	0x0	
63: 61	Reserved	RW	0x0	

4.13

0x0420

0x0420

4- 16^{bit} 0xM

		M		
0	di sabl e_j tag	RW	0x0	JTAG
1	di sabl e_j tag_Core	RW	0x0	JTAG
2	di sabl e_LA132	RW	0x0	LA132
3	di sabl e_j tag_LA132	RW	0x0	LA132 JTAG
4	Di sabl e_anti fuse0	RW	0x0	fuse
5	Di sabl e_anti fuse1	RW	0x0	fuse
6	Di sabl e_I D	RW	0x0	I D
7				
8	resetn_LA132	RW	0x0	LA132
9	sl eepn 7			



63: 0	sram_ctrl	RW	0x0	Sram
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4.16 FUSE0

0x0460

Fuse0

0x0460

4- 19 FUSE

127: 0	Fuse_0	RW	0x0	
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4.17 FUSE1

0x0470

Fuse1

0x0470

4- 20 FUSE

127: 0	Fuse_1	RW	0x0	
--------	--------	----	-----	--

5

3A6000 SYS_CLOCK
 SYS_CLOCK
 3A6000 HT LA132
 0x1fe00000
 I OCSR
 [17: 16]

5.1

SYS_CLOCK 100MHz 25MHz
 CHIP_CONFIG[4]
 HT PHY SYS_CLOCK PHY 200MHz
 CHIP_CONFIG[8] SYS_CLOCK 25MHz
 HT PHY 3.2GHz
 3A6000

5- 1

Boot Clock	SYS_CLOCK SYS_PLL	*1	SPI UART I2C AVS SYS_PLL
Main Clock	Back PLL	PLL	Node Clock Core Clock HTcore Clock LA132 Clock Mem Clock Stable Clock
Node Clock	Main Clock	*1	HT
Core0 Clock	Main Clock	*1	Core0
Core1 Clock	Main Clock	*1	Core1
Core2 Clock	Main Clock	*1	Core2
Core3 Clock	Main Clock	*1	Core3
HTcore Clock	Node Clock	*1	HT

Mem Clock	MEM PLL	PLL			
	Back PLL	/2 /4 /8			

5.2

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5- 3

35: 32	freqscal e_nøde_core	RW	0x0	0: (n+1)/8 1: 1/(n+1)
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5.2.2

3A6000

" "

0x1fe00000

I OCSR

0x0420

5- 4

22	freqscal e_percore	RW	0x0	
23	cl ken_percore	RW	0x0	

freqscal e_percore

1

freqscal e

freqscal e_nøde

cl ken_percore

1

cl ken

3A6000 4 8

0 2 4 6 4

1 3 5 7

4 5 6

7

0x1fe10000

0x1050

5- 5

4	freqscal e_nøde	RW	0x0	0: (n+1)/8 1: 1/(n+1)
3	cl ken	RW	0x0	
2: 0	freqscal e	RW	0x0	



5.4 HT

HT

0x1fe00000

I CCSR

0x0180

5- 8

26: 24	HT_freq_scale_ctrl	RW	3' b111	HT
27	HT_clken	RW	1' b1	HT

HT



GPI_O_FUNC_en[13] 1 stable counter GPIO[13]
GPIO 0x1fe00000 I OCSR
0x0500

5- 11 GPIO





↓
V
C3

↓
C
↓



7 GPIO

3A6000 20 GPIO

GPIO

0x1fe0000

7.1

0x0500

0x1fe0000

0x0500

7- 1

31: 0	GPIO_CEn	RW	32' hfffffff	GPIO
63: 32	GPIO_FUNC_En	RW	32' hffff0000	GPIO

7.2

0x0508

0x1fe0000

0x0508

7- 2





7.4 GPIO



7.5 GPIO

3A6000 GPIO

GPIO0 GPIO08 GPIO16 0

GPIO1 GPIO09 GPIO17 1

GPIO2 GPIO10 GPIO18 2

GPIO3 GPIO11 GPIO19 3

GPIO4 GPIO12 4

GPIO5 GPIO13 5

GPIO6 GPIO14 6

GPIO7 GPIO15 7

GPIO20- GPIO31

GPIO

GPIO_I_NT_en

GPIO_I_NT_PCL

0x1fe00000

0x0510

7- 5

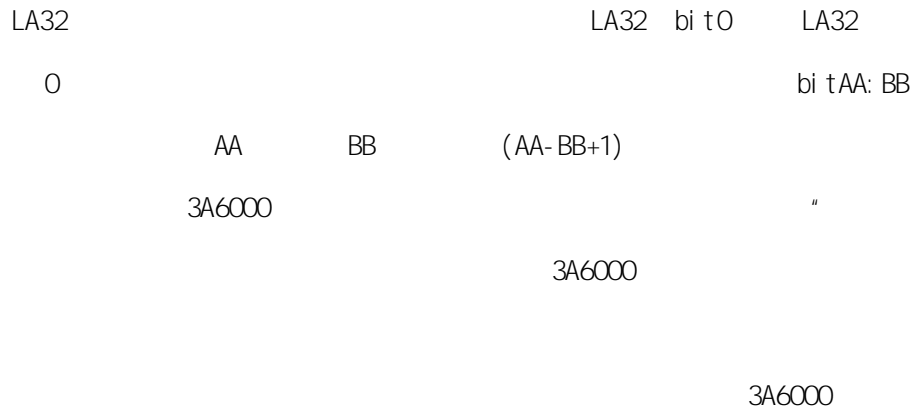
31: 0	GPIO_I_NT_Pol	RW	32' h0	GPIO 0 - 1 -
63: 32	GPIO_I_NT_en	RW	32' h0	GPIO

GPIO

PCL 0

1





8- 1

0x0	31: 0	PRI d		32' h14_d001
0x1	1: 0	ARCH	2' b00 LA32 2' b01 LA32 2' b10 LA64 2' b11	2' b10
	2	PGMMU	1 MMU	1' b1
	3	I OCSR	1 I OCSR	1' b1
	11: 4	PALEN	PALEN 1	8' d47
	19: 12	VALEN	VALEN 1	8' d47
	20	UAL	1	1' b1
	21	RI	1 " "	1' b1
	22	EP	1 " "	1' b1
	23	RPLV	1 RPLV	1' b1
	24	HP	1 huge page	1' b1
	25	CRC32	1 CRC32	1' b1
	26	M&G_I NT	1	1' b1
	0x2	0	FP	1
1		FP_SP	1	1' b1
2		FP_DP	1	1' b1
5: 3		FP_ver	1 I EEE 754- 2008	3' h1
6		LSX	1 128	1' b1
7		LASX	1 256	1' b1
14		LLFTP	1	1' b1



	17: 15	LLFTP_ver		1		3'	h1	
	21	LSPW		1		1'	b1	
	22	LAM		1	AM	1'	b1	
	0	CCDMA		1	Cache Coherent DMA	1'	b1	
	1	SFB		1	Store Fill Buffer SFB	1'	b1	
	3	LLEXC		1	LL	1'	b1	
	4	SCDLY		1	SC	1'	b1	
	5	LLDBAR		1	LL dbar	1'	b1	
Ox3	6	ITLBHMC		1	ITLB TLB	1'	b1	
	7	ICHMC		1	I Cache	1'	b1	
					DCache			
	10: 8	SPW_LVL			page wal k	3'	h4	
	11	SPW_HP_HF		1	page wal k TLB	1'	b1	
	12	RVA		1		1'	b1	
	16: 13	RVMAX-1			-1	4'	h7	
Ox4	31: 0	CC_FREQ			Hz		N/A	
	15: 0	CC_MUL					N/A	
Ox5	31: 16	CC_DIV					N/A	
	0	PMP		1		1'	b1	
	3: 1	PWER			1	3'	h1	
Ox6	7: 4	PNUM			-1	4'	h3	
	13: 8	PMBLTS			-1	6'	h3f	
	14	UPM		1		1'	b1	
	0	L1 IU_Present		1	Cache	Cache	1'	b1
	1	L1 IU_Uni fy		1	L1 IU_Present	Cache	1'	b0
					Cache			
	2	L1 D_Present		1	Cache		1'	b1
	3	L2 IU_Present		1	Cache	Cache	1'	b1
Ox10	4	L2 IU_Uni fy		1	L2 IU_Present	Cache	1	
					Cache			
	5	L2 IU_Pri vate		1	L2 IU_Present	Cache	1	
	6	L2 IU_Incl usi ve		1	L2 IU_Present	Cache	1	



		L1			
7	L2 D Present	1	Cache		1' b0
8	L2 D Pri vate	1	Cache	i	



3A6000

8.2 3A 6000

3A6000 I OCSR

I OCSR TAG

I OCSR I OCSR RD. B/H/W/D I OCSR WR. B/H/W/D

I OCSR RD. B/H/W/D I OCSR RD. B/H/W/D rd, rj rj

I OCSR I OCSR rd I OCSR WR. B/H/W/D

I OCSR WR. B/H/W/D rd, rj W rj I OCSR

rd I OCSR I OCSR RD. B/H/W/D d, D

I OCSR RD. B/H/W/D D d, D



9 Cache SCache

SCache

3A6



3A6000

Sl ock2_mask	0x0250	[47: 0]	2
Sl ock3_val i d	0x0218	[63: 63]	3
Sl ock3_addr	0x0218		



3A6000

	en			
36	MCC clean shared replacement	RW	1' b0	



10

3A6000 8 I PI BI OS

3A6000

10.1

3A6000 0x1fe00000
I OCSR 0x3ff00000

di sabl e_0x3ff0 10- 1 10- 5

3A6000 8 3

8

[17: 16] 4 7 0x1fe10000

0 3

10- 1

I PI _Status	R	32	1	INT4
I PI _Enabl e	RW	32		
I PI _Set	W	32	1	STATUS 1
I PI _Cl ear	W	32	1	STATUS 0
Ma i l Box0	RW		64 32	uncache
Ma i l Box01	RW		64 32	uncache
Ma i l Box02	RW		64 32	uncache
Ma i l Box03	RW		64 32	uncache

3A6000

10- 2 0

Core0_I PI _Status	0x1000	R	0	I PI _Status
Core0_I PI _Enal be	0x1004	RW	0	I PI _Enal be



Core0_IPI_Set	0x1008	W	0	IPI_Set
Core0_IPI_Clear	0x100c	W	0	IPI_Clear
Core0_MailBox0	0x1020	RW	0	IPI_MailBox0
Core0_MailBox1	0x1028	RW	0	IPI_MailBox1
Core0_MailBox2	0x1030	RW	0	IPI_MailBox2
Core0_MailBox3	0x1038	RW	0	IPI_MailBox3

10- 3 1

Core1_IPI_Status	0x1100	R	1	IPI_Status
Core1_IPI_Enable	0x1104	RW	1	IPI_Enable
Core1_IPI_Set	0x1108	W	1	IPI_Set
Core1_IPI_Clear	0x110c	W	1	IPI_Clear
Core1_MailBox0	0x1120	R	1	IPI_MailBox0
Core1_MailBox1	0x1128	RW	1	IPI_MailBox1
Core1_MailBox2	0x1130	W	1	IPI_MailBox2
Core1_MailBox3	0x1138	W	1	IPI_MailBox3

10- 4 2

Core2_IPI_Status	0x1200	R	2	IPI_Status
Core2_IPI_Enable	0x1204	RW	2	IPI_Enable
Core2_IPI_Set	0x1208	W	2	IPI_Set
Core2_IPI_Clear	0x120c	W	2	IPI_Clear
Core2_MailBox0	0x1220	R	2	IPI_MailBox0
Core2_MailBox1	0x1228	RW	2	IPI_MailBox1
Core2_MailBox2	0x1230	W	2	IPI_MailBox2
Core2_MailBox3	0x1238	W	2	IPI_MailBox3

10- 5 3

Core3_IPI_Status	0x1300	R	3	IPI_Status
Core3_IPI_Enable	0x1304	RW	3	IPI_Enable
Core3_IPI_Set	0x1308	W	3	IPI_Set
Core3_IPI_Clear	0x130c	W	3	IPI_Clear
Core3_MailBox0	0x1320	R	3	IPI_MailBox0
Core3_MailBox1	0x1328	RW	3	IPI_MailBox1
Core3_MailBox2	0x1330	W	3	IPI_MailBox2
Core3_MailBox3	0x1338	W	3	IPI_MailBox3

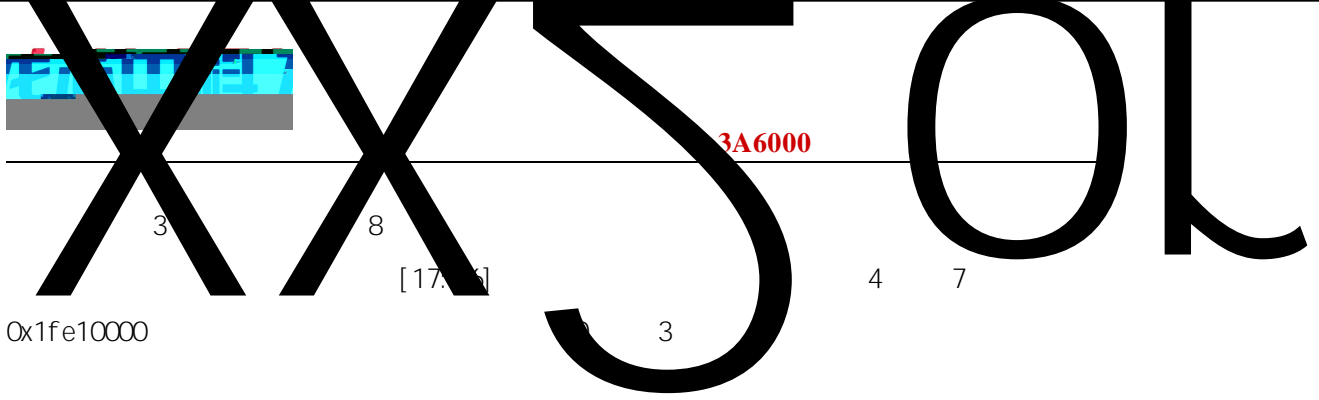
3A6000

0

3

3A6000

8



0x1fe10000

10.2

3A6000

10- 6

		sLE	
perCore_IPI_Status	0x1000	R	IPI_Status
perCore_IPI_Enalbe	0x1004	RW	IPI_Enalbe
perCore_IPI_Set	0x1008	W	IPI_Set
perCore_IPI_Clear	0x100c	W	IPI_Clear
perCore_MailBox0	0x1020	RW	IPI_MailBox0
perCore_MailBox1	0x1028	RW	IPI_MailBox1
perCore_MailBox2	0x1030	RW	IPI_MailBox2
perCore_MailBox3	0x1038	RW	IPI_MailBox3

MailBox

bego e



			0 - Mail Box0 32 1 - Mail Box0 32 2 - Mail Box1 32 3 - Mail Box1 32 4 - Mail Box2 32 5 - Mail Box2 32 6 - Mail Box3 32 7 - Mail Box4 32 [1: 0]
FREQ_Send	0x1058	WD	32 [31] 1 [30: 27] mask 32 1000b 0-2 0000b 0-3 [26] [25: 16] [15: 5] [4: 0] I CCSR[0x1050]

Mail_Send

32

64

Mail_Box

Mail_Box

10.3

IPI_Send Mail_Send Freq_Send

Any_Send

10- 8

ANY_Send	0x1158	WD	64 [63: 32] [31] 1 [30: 27] mask 32 1000b 0-2 0000b 0-3 [26]
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3A6000

		[25: 16] [15: 0]
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11 I/O

3A6000

I/O

HT

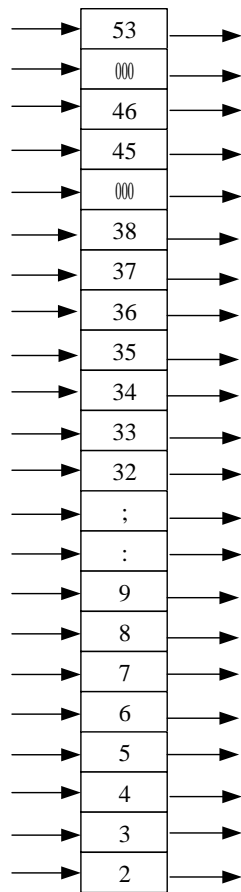
3A6000

11.1 I/O

3A6000

32

I/O



KR2
KR3
KR4
KR5



	Enable		Intenset	Intencl r	Inten	Intenset
	Intenset	1		Intencl r		
Intencl r	1		Inten			
		Intedge			1	0
		Intencl r				

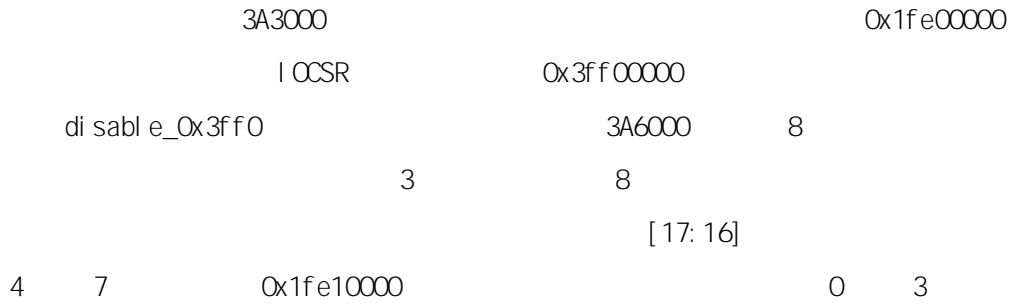
11- 1

	Intedge	Inten	Intenset	Intencl r	
0	RW/ 0	R / 0	RW/ 0	RW/ 0	GPI 024/16/8/0/SC0
1	RW/ 0	R / 0	RW/ 0	RW/ 0	GPI 025/17/9/1/SC1
2	RW/ 0	R / 0	RW/ 0	RW/ 0	GPI 026/18/10/2/SC2
3	RW/ 0	R / 0	RW/ 0	RW/ 0	GPI 027/19/11/3/SC3
4	RW/ 0	R / 0	RW/ 0	RW/ 0	GPI 028/20/12/4
5	RW/ 0	R / 0	RW/ 0	RW/ 0	GPI 029/21/13/5
6	RW/ 0	R / 0	RW/ 0	RW/ 0	GPI 030/22/14/6
7	RW/ 0	R / 0	RW/ 0	RW/ 0	GPI 031/23/15/7
8	RW/ 0	R / 0	RW/ 0		

1
 47
 6
 TP
 S
 TP
 [e @ x i n x s o



11.1.1



11- 2 IO



Inti sr	0x1420	32	
Inten	0x1424	32	
Intenset	0x1428	32	
Intencl r	0x142c	32	
Intedge	0x1434	32	
CORE0_ J NTI SR	0x1440		CORE0 32
CORE1_ J NTI SR	0x1448		CORE1 32
CORE2_ J NTI SR	0x1450		CORE2 32
CORE3_ J NTI SR	0x1458		CORE



11- 4

Entry0	0x1400	GPI 024/16/8/0	Entry16	0x1410	
Entry1	0x1401	GPI 025/17/9/1	Entry17	0x1411	
Entry2	0x1402	GPI 026/18/10/2	Entry18	0x1412	
Entry3	0x1403	GPI 027/19/11/3	Entry19	0x1413	
Entry4	0x1404	GPI 028/20/12/4	Entry20	0x1414	
Entry5	0x1405	GPI 029/21/13/5	Entry21	0x1415	
Entry6	0x1406	GPI 030/22/14/6	Entry22	0x1416	
Entry7	0x1407	GPI 031/23/15/7	Entry23	0x1417	
Entry8	0x1408	I 2C0	Entry24	0x1418	HT1-i nt0
Entry9	0x1409	I 2C1	Entry25	0x1419	HT1-i nt1
Entry10	0x140a	UART0	Entry26	0x141a	HT1-i nt2
Entry11	0x140b	MCO	Entry27	0x141b	HT1-i nt3
Entry12	0x140c	MC1/AVS	Entry28	0x141c	HT1-i nt4
Entry13	0x140d	SPI	Entry29	0x141d	HT1-i nt5
Entry14	0x140e	Thsens	Entry30	0x141e	HT1-i nt6
Entry15	0x140f	UART1	Entry31	0x141f	HT1-i nt7

11.1.2

3A6000

11- 5

per Core_I NTI SR	0x1010	32
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11.2 I/O

256 I/O 3A6000 I/O HT
HT I/O



IO " "
Ox1fe0000 IOCSR Ox0420

11- 6

Table with 5 columns: bit width (48), register name (EXT_INT_en), access type (RW), value (0x0), and I/O type (IO)

IO HT
256

11.2.1

IO
Ox1fe0000 3A6000
8 3 8
[17: 16]
4 7 Ox1fe10000
0 3

11- 7 IO

Table with 4 columns: register name (EXT_ID en), address (0x1600, 0x1608, 0x1610), I/O type (IO), and bit range ([63: 0], [127: 64], [191: 128])



11- 10



EXT_IQ map3	0x14C3	EXT_IQ [127: 96]
EXT_IQ map4	0x14C4	EXT_IQ [159: 128]
EXT_IQ map5	0x14C5	EXT_IQ [191: 160]
EXT_IQ map6	0x14C6	EXT_IQ [223: 192]
EXT_IQ map7	0x14C7	EXT_IQ [255: 224]

11- 14 [7: 4] 8 11- 13
 11- 14 [7: 4] 11- 15
 0x48 EXT_IQ _node_type4 3

11- 13

3: 0	
7: 4	11- 15

EXT_IQ bounce 1

EXT_IQ bounce

11- 13 0x27 11- 15 EXT_IQ _node_type2
 0 0 0 1 0 2
 1 0 1 1 1 2 4 0 4 1 4 2
 EXT_IQ bounce 0 bi tmap
 1 0

11- 14

EXT_IQ map_Core0	0x1C00	EXT_IQ [0]
EXT_IQ map_Core1	0x1C01	EXT_IQ [1]
EXT_IQ map_Core2	0x1C02	EXT_IQ [2]
EXT_IQ map_Core254	0x1CFE	EXT_IQ [254]
EXT_IQ map_Core255	0x1CFF	EXT_IQ [255]

11- 15

EXT_IQ _node_type0	0x14A0	16	0
EXT_IQ _node_type1	0x14A2	16	1
EXT_IQ _node_type2	0x14A4	16	2



EXT_ID_node_type15	0x14BE	16	15

11.2.2

11- 16

IO

per Core_EXT_ID_sr [63: 0]	0x1800	IO [63: 0]
per Core_EXT_ID_sr [127: 64]	0x1808	IO [127: 64]
per Core_EXT_ID_sr [191: 128]	0x1810	IO [191: 128]
per Core_EXT_ID_sr [255: 192]	0x1818	IO [255: 192]

11.2.3 IO

IO
IO

IO

11- 17 IO

EXT_ID_send	0x1140	W0	IO [7: 0]

11.2.4 IO HT

HT HT HT HT

256 256 4 8

HT IO

8

IO HT HT



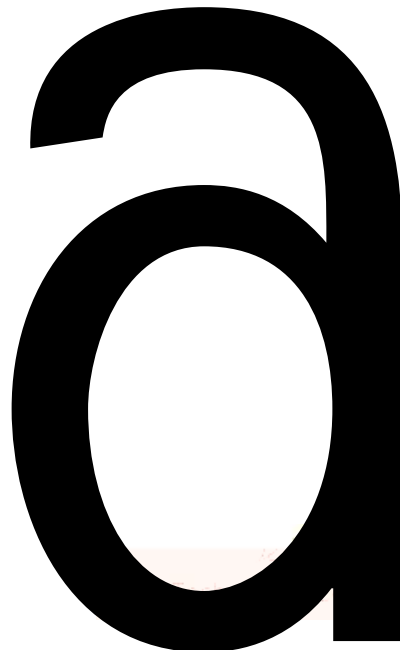
3A6000

12

12.1

3A6000

Ox1fe00198 g



3A600

1

3A6000

2

0 1

4

0x

12- 3



These

0x1460

RW

7:

ngson



[7: 0]	Scal e_gate0	0
[8: 8]	Scal e_en0	0
[11: 10]	Scal e_Sel 0	0
[14: 12]	Scal e_freq0	
[23: 16]	Scal e_gate1	1
[24: 24]	Scal e_en1	1
[27: 26]	Scal e_Sel 1	1
[30: 28]	Scal e_freq1	
[39: 32]	Scal e_gate2	2
[40: 40]	Scal e_en2	2
[43: 42]	Scal e_Sel 2	2
[46: 44]	Scal e_freq2	
[55: 48]		

Thsens_freq_scal e 0x1480 RW



11: 9	Temp_cl uster	RW	0	Thsens_tri gger

12- 7

3	Out_mode	R	0	0 1
6: 4	Out_cl uster	R	0	
7	Overfl ow	R	0	
29: 16	Data	R	0	

$\text{=data} * 820 / 0x4000 - 311$ $-40 \quad -125$
 $\text{=}(data+110) * 1.226 / 0x1000$

3A6000

Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0
0x0000							version(RD)	
0x0008		sw_tch_byte48	x4_mode	ddr3_mode			capability RD	
0x0010							dram_init(RD)	init_start
0x0018								
0x0020							preamble2	rdifo_val id
0x0028		rdifo_empty(RD)				Overflow(RD)		
0x0030		dll_val ue(RD)	dll_i nit_done(RD)	dll_l ock_mode	dll_bypass	dll_adj _cnt	dll_i ncrement	dll_start_poi nt
0x0038				dll_dbl _fi x			dll_cl ose_di sabl e	dll_ck
0x0040								
0x0048							cl ken_ckca	
0x0050								
0x0058							cl ken_ds_0	
0x0060								
0x0068							cl ken_ds_1	
0x0070								
0x0078								



Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0
0x0110	rdodt_ctrl_0	rdgate_l_en_0	rdgate_mode_0	rdgate_ctrl_0			dqs_oe_ctrl_0	dq_oe_ctrl_0
0x0118				odt_l_en_add_0		dl_y_2x_0	redge_sel_0	rddqs_phase_0(RD)
0x0120	w_bdl_y0_0[31: 28]	w_bdl_y0_0[27: 24]	w_bdl_y0_0[23: 20]	w_bdl_y0_0[19: 16]	w_bdl_y0_0[15: 12]	w_bdl_y0_0[11: 8]	w_bdl_y0_0[7: 4]	w_bdl_y0_0[3: 0]
0x0128		w_bdl_y0_0[59: 56]	w_bdl_y0_0[55: 52]	w_bdl_y0_0[51: 48]	w_bdl_y0_0[47: 44]	w_bdl_y0_0[43: 40]	w_bdl_y0_0[39: 36]	w_bdl_y0_0[35: 32]
0x0130	w_bdl_y1_0[24: 21]	w_bdl_y1_0[20: 18]	w_bdl_y1_0[17: 15]	w_bdl_y1_0[14: 12]	w_bdl_y1_0[11: 9]	w_bdl_y1_0[8: 6]	w_bdl_y1_0[5: 3]	w_bdl_y1_0[2: 0]
0x0138								w_bdl_y1_0[27: 26]
0x0140							rg_bdl_y_0[7: 4]	rg_bdl_y_0[3: 0]
0x0148								
0x0150	rdqsp_bdl_y_0[31: 28]	rdqsp_bdl_y_0[27: 24]	rdqsp_bdl_y_0[23: 20]	rdqsp_bdl_y_0[19: 16]	rdqsp_bdl_y_0[15: 12]	rdqsp_bdl_y_0[11: 8]	rdqsp_bdl_y_0[7: 4]	rdqsp_bdl_y_0[3: 0]
0x0158								rdqsp_bdl_y_0[35: 32]
0x0160	rdqsn_bdl_y_0[31: 28]	rdqsn_bdl_y_0[27: 24]	rdqsn_bdl_y_0[23: 20]	rdqsn_bdl_y_0[19: 16]	rdqsn_bdl_y_0[15: 12]	rdqsn_bdl_y_0[11: 8]	rdqsn_bdl_y_0[7: 4]	rdqsn_bdl_y_0[3: 0]
0x0168								rdqsn_bdl_y_0[35: 32]
0x0170	rdq_bdl_y_0[24: 21]	rdq_bdl_y_0[20: 18]	rdq_bdl_y_0[17: 15]	rdq_bdl_y_0[14: 12]	rdq_bdl_y_0[11: 9]	rdq_bdl_y_0[8: 6]	rdq_bdl_y_0[5: 3]	rdq_bdl_y_0[2: 0]
0x0178								rdq_bdl_y_0[27: 26]
0x0180					dl_l_1xdl_y_1	dl_l_1xgen_1	dl_l_vrdqs_1	dl_l_vrdq_1
0x0188		vref_sample_1	vref_clk_inv_1	dl_l_vref_1	vref_dl_y_1	dl_l_gate_1	dl_l_rddqs_1	dl_l_rddqs0_1
0x0190	rdodt_ctrl_1	rdgate_l_en_1	rdgate_mode_1	rdgate_ctrl_1			dqs_oe_ctrl_1	dq_oe_ctrl_1
0x0198				odt_l_en_add_1		dl_y_2x_1	redge_sel_1	rddqs_phase_1(RD)
0x01a0	w_bdl_y0_1[31: 28]	w_bdl_y0_1[27: 24]	w_bdl_y0_1[23: 20]	w_bdl_y0_1[19: 16]	w_bdl_y0_1[15: 12]	w_bdl_y0_1[11: 8]	w_bdl_y0_1[7: 4]	w_bdl_y0_1[3: 0]
0x01a8		w_bdl_y0_1[59: 56]	w_bdl_y0_1[55: 52]	w_bdl_y0_1[51: 48]	w_bdl_y0_1[47: 44]	w_bdl_y0_1[43: 40]	w_bdl_y0_1[39: 36]	w_bdl_y0_1[35: 32]
0x01b0	w_bdl_y1_1[24: 21]	w_bdl_y1_1[20: 18]	w_bdl_y1_1[17: 15]	w_bdl_y1_1[14: 12]	w_bdl_y1_1[11: 9]	w_bdl_y1_1[8: 6]	w_bdl_y1_1[5: 3]	w_bdl_y1_1[2: 0]
0x01b8								w_bdl_y1_1[27: 26]
0x01c0							rg_bdl_y_1[7: 4]	rg_bdl_y_1[3: 0]
0x01c8								
0x01d0	rdqsp_bdl_y_1[31: 28]	rdqsp_bdl_y_1[27: 24]	rdqsp_bdl_y_1[23: 20]	rdqsp_bdl_y_1[19: 16]	rdqsp_bdl_y_1[15: 12]	rdqsp_bdl_y_1[11: 8]	rdqsp_bdl_y_1[7: 4]	rdqsp_bdl_y_1[3: 0]
0x01d8								rdqsp_bdl_y_1[35: 32]
0x01e0	rdqsn_bdl_y_1[31: 28]	rdqsn_bdl_y_1[27: 24]	rdqsn_bdl_y_1[23: 20]	rdqsn_bdl_y_1[19: 16]	rdqsn_bdl_y_1[15: 12]	rdqsn_bdl_y_1[11: 8]	rdqsn_bdl_y_1[7: 4]	rdqsn_bdl_y_1[3: 0]
0x01e8								rdqsn_bdl_y_1[35: 32]
0x01f0	rdq_bdl_y_1[24: 21]	rdq_bdl_y_1[20: 18]	rdq_bdl_y_1[17: 15]	rdq_bdl_y_1[14: 12]	rdq_bdl_y_1[11: 9]	rdq_bdl_y_1[8: 6]	rdq_bdl_y_1[5: 3]	rdq_bdl_y_1[2: 0]
0x01f8								rdq_bdl_y_1[27: 26]
0x0200					dl_l_1xdl_y_2	dl_l_1xgen_2	dl_l_vrdqs_2	dl_l_vrdq_2
0x0208		vref_sample_2	vref_clk_inv_2	dl_l_vref_2	vref_dl_y_2	dl_l_gate_2	dl_l_rddqs_2	dl_l_rddqs0_2
0x0210	rdodt_ctrl_2	rdgate_l_en_2	rdgate_mode_2	rdgate_ctrl_2			dqs_oe_ctrl_2	dq_oe_ctrl_2



3A6000

Offset



3A6000

Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0
0x0320	w_bdl y0_4[31: 28]	w_bdl y0_4[27: 24]	w_bdl y0_4[23: 20]	w_bdl y0_4[19: 16]	w_bdl y0_4[15: 12]	w_bdl y0_4[11: 8]	w_bdl y0_4[7: 4]	w_bdl y0_4[3: 0]
0x0328		w_bdl y0_4[59: 56]	w_bdl y0_4[55: 52]	w_bdl y0_4[51: 48]	w_bdl y0_4[47: 44]	w_bdl y0_4[43: 40]	w_bdl y0_4[39: 36]	w_bdl y0_4[35: 32]
0x0330	w_bdl y1_4[24: 21]	w_bdl y1_4[20: 18]	w_bdl y1_4[17: 15]	w_bdl y1_4[14: 12]	w_bdl y1_4[11: 9]	w_bdl y1_4[8: 6]	w_bdl y1_4[5: 3]	w_bdl y1_4[2: 0]
0x0338								w_bdl y1_4[27: 26]
0x0340							rg_bdl y_4[7: 4]	rg_bdl y_4[3: 0]
0x0348								
0x0350	rdqsp_bdl y_4[31: 28]	rdqsp_bdl y_4[27: 24]	rdqsp_bdl y_4[23: 20]	rdqsp_bdl y_4[19: 16]	rdqsp_bdl y_4[15: 12]	rdqsp_bdl y_4[11: 8]	rdqsp_bdl y_4[7: 4]	rdqsp_bdl y_4[3: 0]
0x0358								rdqsp_bdl y_4[35: 32]
0x0360	rdqsn_bdl y_4[31: 28]	rdqsn_bdl y_4[27: 24]	rdqsn_bdl y_4[23: 20]	rdqsn_bdl y_4[19: 16]	rdqsn_bdl y_4[15: 12]	rdqsn_bdl y_4[11: 8]	rdqsn_bdl y_4[7: 4]	rdqsn_bdl y_4[3: 0]
0x0368								rdqsn_bdl y_4[35: 32]
0x0370	rdq_bdl y_4[24: 21]	rdq_bdl y_4[20: 18]	rdq_bdl y_4[17: 15]	rdq_bdl y_4[14: 12]	rdq_bdl y_4[11: 9]	rdq_bdl y_4[8: 6]	rdq_bdl y_4[5: 3]	rdq_bdl y_4[2: 0]
0x0378								rdq_bdl y_4[27: 26]
0x0380					dli_1xdl y_5	dli_1xgen_5		

L 7





3A6000

Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0
0x0428		w_bdl y0_6[59: 56]	w_bdl y0_6[55: 52]	w_bdl y0_6[51: 48]	w_bdl y0_6[47: 44]	w_bdl y0_6[43: 40]	w_bdl y0_6[39: 36]	w_bdl y0_6[35: 32]
0x0430	w_bdl y1_6[24: 21]	w_bdl y1_6[20: 18]	w_bdl y1_6[17: 15]	w_bdl y1_6[14: 12]	w_bdl y1_6[11: 9]	w_bdl y1_6[8: 6]	w_bdl y1_6[5: 3]	w_bdl y1_6[2: 0]
0x0438								w_bdl y1_6[27: 26]
0x0440							rg_bdl y_6[7: 4]	rg_bdl y_6[3: 0]
0x0448								
0x0450	rdqsp_bdl y_6[31: 28]	rdqsp_bdl y_6[27: 24]	rdqsp_bdl y_6[23: 20]	rdqsp_bdl y_6[19: 16]	rdqsp_bdl y_6[15: 12]	rdqsp_bdl y_6[11: 8]	rdqsp_bdl y_6[7: 4]	rdqsp_bdl y_6[3: 0]
0x0458								rdqsp_bdl y_6[35: 32]
0x0460	rdqsn_bdl y_6[31: 28]	rdqsn_bdl y_6[27: 24]	rdqsn_bdl y_6[23: 20]	rdqsn_bdl y_6[19: 16]	rdqsn_bdl y_6[15: 12]	rdqsn_bdl y_6[11: 8]	rdqsn_bdl y_6[7: 4]	rdqsn_bdl y_6[3: 0]
0x0468								rdqsn_bdl y_6[35: 32]
0x0470	rdq_bdl y_6[24: 21]	rdq_bdl y_6[20: 18]	rdq_bdl y_6[17: 15]	rdq_bdl y_6[14: 12]	rdq_bdl y_6[11: 9]	rdq_bdl y_6[8: 6]	rdq_bdl y_6[5: 3]	rdq_bdl y_6[2: 0]
0x0478								rdq_bdl y_6[27: 26]
0x0480					dl l _1xdl y_7	dl l _1xgen_7	dl l _wr dq_7	dl l _wr dq_7
0x0488		vref_sampl e_7	vref_cl k_i nv_7	dl l _vref_7	vref_dl y_7	dl l _gate_7	dl l _rdq_7	dl l _rdq_7
0x0490	rdodt_ctrl _7	rdgate_l en_7	rdgate_node_7	rdgate_ctrl _7			dqs_oe_ctrl _7	dq_oe_ctrl _7
0x0498				odt_l en_add_7		dl y_2x_7	redge_sel _7	rdq_phase_7(RD)
0x04a0	w_bdl y0_7[31: 28]	w_bdl y0_7[27: 24]	w_bdl y0_7[23: 20]	w_bdl y0_7[19: 16]	w_bdl y0_7[15: 12]	w_bdl y0_7[11: 8]	w_bdl y0_7[7: 4]	w_bdl y0_7[3: 0]
0x04b8								w_bdl y1_7[27: 26]
0x04c0							rg_bdl y_7[7: 4]	rg_bdl y_7[3: 0]
0x04c8								
0x04d0	rdqsp_bdl y_7[31: 28]	rdqsp_bdl y_7[27: 24]	rdqsp_bdl y_7[23: 20]	rdqsp_bdl y_7[19: 16]	rdqsp_bdl y_7[15: 12]	rdqsp_bdl y_7[11: 8]	rdqsp_bdl y_7[7: 4]	rdqsp_bdl y_7[3: 0]
0x04d8								rdqsp_bdl y_7[35: 32]
0x04e0	rdqsn_bdl y_7[31: 28]	rdqsn_bdl y_7[27: 24]	rdqsn_bdl y_7[23: 20]	rdqsn_bdl y_7[19: 16]	rdqsn_bdl y_7[15: 12]	rdqsn_bdl y_7[11: 8]	rdqsn_bdl y_7[7: 4]	rdqsn_bdl y_7[3: 0]
0x04e8								rdqsn_bdl y_7[35: 32]
0x04f0	rdq_bdl y_7[24: 21]	rdq_bdl y_7[20: 18]	rdq_bdl y_7[17: 15]	rdq_bdl y_7[14: 12]	rdq_bdl y_7[11: 9]	rdq_bdl y_7[8: 6]	rdq_bdl y_7[5: 3]	rdq_bdl y_7[2: 0]
0x04f8								rdq_bdl y_7[27: 26]
0x0500					dl l _1xdl y_8	dl l _1xgen_8	dl l _wr dq_8	dl l _wr dq_8
0x0508		vref_sampl e_8	vref_cl k_i nv_8	dl l _vref_8	vref_dl y_8	dl l _gate_8	dl l _rdq_8	dl l _rdq_8
0x0510	rdodt_ctrl _doate_8e_							



	53: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0
CTL								
0x1000	tMRD	tRP	tWLDQSEN	tMOD	tXPR		tCKE	tRESET
0x1008								tODTL
0x1010	tREFretention				tRFC		tREF	
0x1018	tCKESR	tXSRD	tXS		tRFC_dlr			tREF_IDLE
0x1020								





3A6000

Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: - 4
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3A6000

Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0	
0x1260	retry_cnt (RD)					rbuffer_max (RD)		rdifo_depth	stat_en
0x1268	pmrdage_low		pmrdage_up		pmpref_near_full	pmhot_en	pmhot_minus	pmhot_count	
0x1270	pmstb_error (RD)			pmstb_deb_cnt_sel	pmstb_dbg_cnt				
0x1278	pmstb_adj_ust				pmstb_di_stance	stb_context_gnt	pmstb_col_d_time		
0x1280	aw_512_al_ign		rd_before_wr	ecc_enable		int_vector (RD)	int_trigger (RD)	int_enable	
0x1288	pmstb_arpri_or_cfg								
0x1290	i								



! 0F





3A6000

Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0
0x13d0	odt_rd_cs_map							



3A6000

Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0
0x1580	w n0_mask							
0x1588	w n1_mask							
0x1590	w n2_mask							
0x1598	w n3_mask							
0x15a0	w n4_mask							
0x15a8	w n5_mask							
0x15b0	w n6_mask							
0x15b8	w n7_mask							
0x1600	w n0_rmap							
0x1608	w n1_rmap							
0x1610	w n2_rmap							
0x1618	w n3_rmap							
0x1620	w n4_rmap							
0x1628	w n5_rmap							
0x1630	w n6_rmap							
0x1638	w n7_rmap							
0x1680	w i te_trai n_data[63: 0]							
0x1688	w i te_trai n_data[127: 64]							
0x1690	w i te_trai n_data[191: 128]							
0x1698	w i te_trai n_data[255: 192]							
0x16a0	w i te_trai n_data[319: 256]							
0x16a8	w i te_trai n_data[383: 320]							
0x16b0	w i te_trai n_data[447: 384]							
0x16b8	w i te_trai n_data[511: 448]							
0x16c0	w i te_trai n_ecc_data[63: 0]							
0x16c8		trai n_wi te_n	obj_addr		trai n_ecc_cmt_en		rw_trai n_req	rw_trai n_mode
0x1700							acc_hp	acc_en
0x1708	acc_fake_b				acc_fake_a			
0x1710								



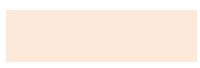
3A6000

Offset

UUI 30

36000

Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0	
0x21a8	cs_turnaround (RO)								
0x21b0	bg_conflict (RO)								
0x2300						sm_leveling	sm_init		
0x2308									
0x2310	sm_rank_03		sm_rank_02		sm_rank_01		sm_rank_00		
0x2318	sm_rank_07		sm_rank_06		sm_rank_05		sm_rank_04		
0x2320	sm_rank_11		sm_rank_10		sm_rank_09		sm_rank_08		
0x2328	sm_rank_15		sm_rank_14		sm_rank_13		sm_rank_12		
0x2330	sm_rank_19		sm_rank_18		sm_rank_17		sm_rank_16		
0x2338	sm_rank_23		sm_rank_22		sm_rank_21		sm_rank_20		
0x2340	sm_rank_27		sm_rank_26		sm_rank_25		sm_rank_24		
0x2348	sm_rank_31		sm_rank_30		sm_rank_29		sm_rank_28		
0x2430	cache_monitor_cnt (RO)								
0x2438	cache_monitor_cnt (RO)								





3A6000

Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0
0x2638	fi_x_r2r_dl_y_count (RO)				fi_x_v2v_dl_y_count (RO)			
0x2640	fi_x_r2v_dl_y_count (RO)				fi_x_v2r_dl_y_count (RO)			
TST								
0x3000						l_pbk_mode		



3A6000

Offset	63: 56	55: 48	47: 40	39: 32	31: 24	23: 16	15: 8	7: 0
0x3178	obs[255: 192] (RO)							
0x3180	obs[319: 256] (RO)							
0x3188	obs[383: 320] (RO)							
0x3190	obs[447: 384] (RO)							
0x3198	obs[511: 448] (RO)							
0x31a0	obs[575: 512] (RO)							
0x31a8	obs[639: 576] (RO)							
0x31b0					obs[671: 640] (RO)			
0x3200								
0x3208								
0x3220	tud_i_0							
0x3228	tud_i_1							
0x3230	tud_o(RO)							
0x3300	tst_300							
0x3308	tst_308							
0x3310	tst_310							
0x3318	tst_318							
0x3320	tst_320							
0x3328	tst_328							
0x3330	tst_330							
0x3338	tst_338							
0x3340	tst_340							
0x3348	tst_348							
0x3350	tst_350							
0x3358	tst_358							
0x3360	tst_360							
0x3368	tst_368							
0x3370	tst_370							
0x3378	tst_378							



13.3

13.3.1

Init_start 0x010 0x2 Init_start

DRAM

- (1) pm_clk_sel_ckca pm_clk_sel_ds
- (2) pm_phy_init_start 1 PHY
- (3) DLL pm_dll_init_done 1
- (4) pm_dll_lock_* pm_pll_lock_* 1
- (5) pm_clken_*
- (6) pm_init_start 1
- (7) pm_dram_init pm_cs_enable

13.3.2

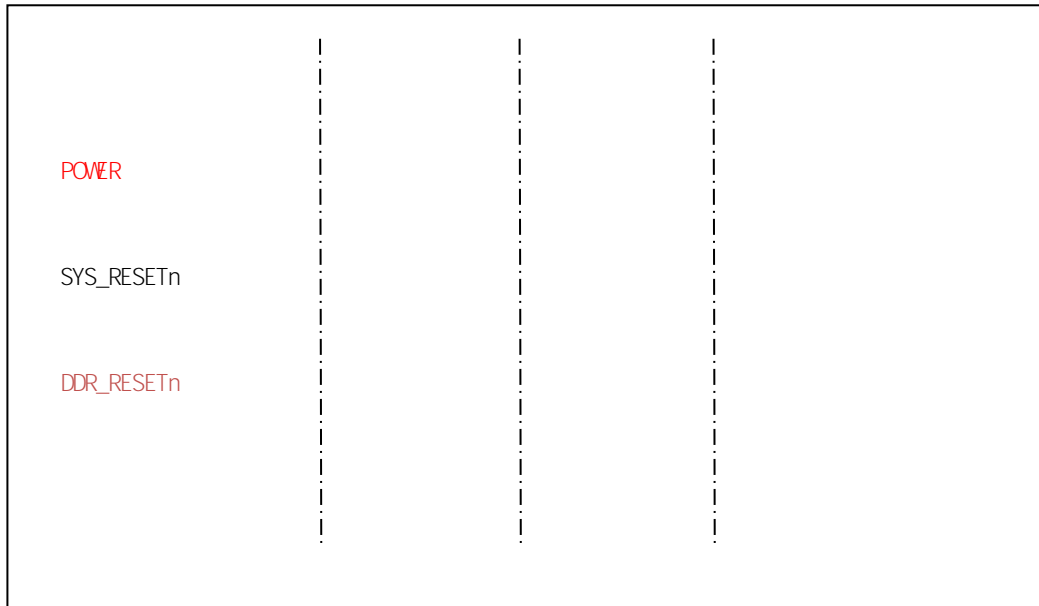
STR pad_reset_po 0x808

DDR_RESETEn

- (1) reset_ctrl[1:0] == 2' b00
DDR_RESETEn

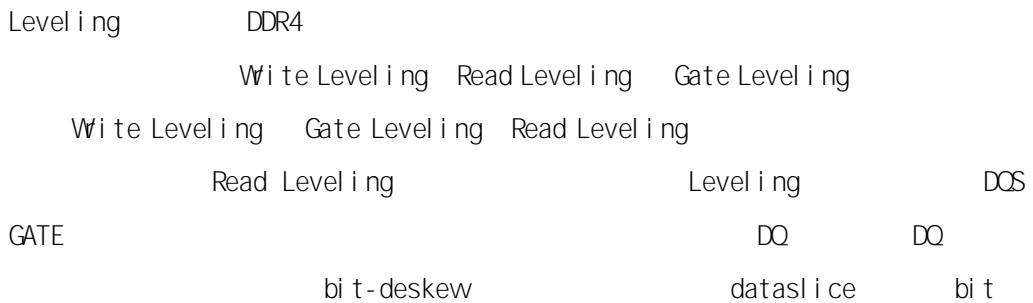


(3) pm_pad_reset_o[1:0] == 2'b01
DDR_RESETn



STR 2
STR 3

13.3.3 Leveling





13.3.3.1 Write Leveling

Write Leveling	DOS			
(1)				
(2)	DI I_wrdqs_x	x = 0 8	0x20	
(3)	DI I_wrdq_x	x = 0 8	0x0	
(4)	Lvl_møde	2' b01		
(5)	Lvl_ready	1		Write Leveling
(6)	Lvl_req	1		
(7)	Lvl_done	1		Write Leveling
(8)	Lvl_resp_x	0		DI I_wrdq_x[6: 0]
	dl I_1xdly[6: 0]	1	5-7	Lvl_resp_x 1 9
	1	DI I_wrdq_x[6: 0]	dl I_1xdly[6: 0]	1 5-7
	Lvl_resp_x	0		DI I_wrdq_x[6: 0] dl I_1xdly[6: 0]
	1	5-7	Lvl_resp_x	1 9
(9)	DI I_wrdq_x	dl I_1xdly	0x40	DI I_wrdq_x dl I_1xdly
(10)	DI MM	pm_dl y_2x	0x0	pm_dl y_2x
	0x010101			
(11)	Lvl_møde	0x700	2' b00	Write Leveling

13.3.3.2 Gate Leveling

Gate Leveling	DOS			
(1)				
(2)	Write Leveling			
(3)	DI I_gate_x	x = 0 8	0	
(4)	Lvl_møde	2' b10		
(5)	Lvl_ready	1		Gate Leveling
(6)	Lvl_req	1		
(7)	Lvl_done	1		Gate Leveling -7



0

(4)	Ms_req	Ox1126	1	DRAM	MRS
(5)	Ms_done	Ox1127		1	MRS

0

(6)



(6) Lpbk_error 1
Lpbk_*
0

13.3.8 ECC

ECC 64
Ecc_enabl e



13- 3 1

1	ECC			1	ECC		
M1_ecc_set		0x0700	RW	[5:0]: M1_int_enable			
				[8]: M1_int_trigger			
				[21:16]: M1_int_vector(RO)			
				[33:32]: M1_ecc_enable ECC			
				[40]: M1_rd_before_w			
		0x0708	RW				
1	ECC			1	ECC		
M1_ecc_cnt		0x0710	RW	[7:0]: M1_int_cnt ECC			
				[15:8]: M1_int_cnt_err(RO) ECC			
				[23:16]: M1_int_cnt_fatal(RO) ECC			
1	ECC			1	ECC		
M1_ecc_cs_cnt		0x0718	RO	[7:0]: M1_ecc_cnt_cs_0 CS0 ECC			
				[15:8]: M1_ecc_cnt_cs_1 CS1 ECC			
				[23:16]: M1_ecc_cnt_cs_2 CS2 ECC			
				[31:24]: M1_ecc_cnt_cs_3 CS3 ECC			
				[39:32]: M1_ecc_cnt_cs_4 CS4 ECC			
				[47:40]: M1_ecc_cnt_cs_5 CS5 ECC			
				[55:48]: M1_ecc_cnt_cs_6 CS6 ECC			
				[63:56]: M1_ecc_cnt_cs_7 CS7 ECC			
1	ECC			1	ECC		
M1_ecc_code		0x0720	RO	[7:0]: M1_ecc_code_64 64 ECC ECC			
				[41:32]: M1_ecc_code_256 256 ECC ECC			
				[52:48]: M1_ecc_code_dir ECC			
				[60:56]: M1_ecc_data_dir ECC			
1	ECC	0x0728	RO	1	ECC		



Mt1_ecc_addr			[63: 0]: Mt1_ecc_addr ECC
1 0 Mt1_ecc_data0	0x0730	RO	1 ECC 0 [63: 0]: Mt1_ecc_data0 ECC 64 ECC 256 ECC [63: 0]
1 1 Mt1_ecc_data1	0x0738	RO	1 ECC 1 [63: 0]: Mt1_ecc_data1 ECC 256 ECC [127: 64]
1 2 Mt1_ecc_data2	0x0740	RO	1 ECC 2 [63: 0]: Mt1_ecc_data2 ECC 256 ECC [191: 128]
1 3 Mt1_ecc_data3	0x0748	RO	1 ECC 3 [63: 0]: Mt1_ecc_data3 ECC 256 ECC [255: 192]



256

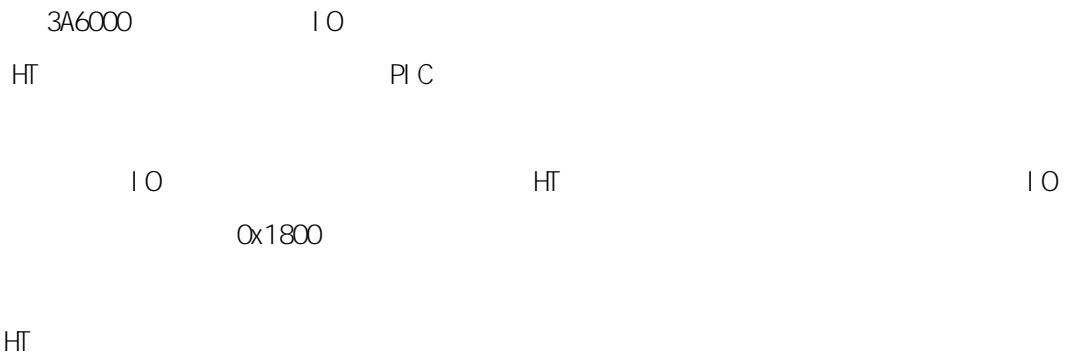
4

PI C

14.3.2



14.3.3



4.1 HyperTransport

3A6000

HyperTransport

14- 5 HyperTransport

0x0E00_0000_0000	0x0EFF_FFFF_FFFF	1 TB	HT
------------------	------------------	------	----

HyperTransport

33. 2

HyperTransport

40

14- 6 3 HyperTransport

0x00_0000_0000	0xFC_FFFF_FFFF	1012 GB	MEM
0xFD_0000_0000	0xFD_0FFF_FFFF	256 MB	
0xFD_1000_0000	0xFD_F7FF_FFFF	3712 MB	
0xFD_F800_0000	0xFD_F8FF_FFFF	16 MB	
0xFD_F900_0000	0xFD_F90F_FFFF	1 MB	PI C
0xFD_F910_0000	0xFD_F91F_FFFF	1 MB	
0xFD_F920_0000	0xFD_FAFF_FFFF	30 MB	
0xFD_FB00_0000	0xFD_FBFF_FFFF	16 MB	HT
0xFD_FC00_0000	0xFD_FDFF_FFFF	32 MB	I/O
0xFD_FE00_0000	0xFD_FFFF_FFFF	32 MB	HT
0xFE_0000_0000	0xFF_FFFF_FFFF	8 GB	



HyperTransport

act_as_slave 1

Post
14. 5. 12

2

HyperTransport
Post Write

Post Write
Post Write HyperTransport

14. 5. 13

2

Cache

IO
HT
HyperTransport



	0x20				
	0x24				
	0x28	Cardbus CIS Pointer			
	0x2c	Subsystem ID		Subsystem Vendor ID	
	0x30	Expansion ROM Enable Address			
	0x34	Reserved		Capabilities Pointer	
	0x38	Reserved			
	0x3c	Bridge Control		Interrupt Pin	Interrupt Line
Cap 0 PRI	0x40	Command		Capabilities Pointer	Capability ID
	0x44	Link Config 0		Link Control 0	
	0x48	Link Config 1		Link Control 1	
	0x4c	LinkFreqCap0		Link Error0/Link Freq 0	Revision ID
	0x50	LinkFreqCap1		Link Error1/Link Freq 1	Feature
	0x54	Error Handling		Enumeration Scratchpad	
	0x58	Reserved		Mem Limit Upper	Mem Enable Upper
Cap 1 Retry	0x60	Capability Type	Reserved	Capability Pointer	Capability ID
	0x64	Status 1	Control 1	Status 0	Control 0
	0x68	Retry Count 1		Retry Count 0	
CAP 3	0x6c	Capability Type	Revision ID	Capability Pointer	Capability ID
CAP 4 Interrupt	0x70	Capability Type	Index	Capability Pointer	Capability ID
	0x74	Dataport			
	0x78	IntrInfo[31: 0]			
	0x7c	IntrInfo[63: 32]			
Int Vector	0x80	INT Vector[31: 0]			
	0x84	INT Vector[63: 32]			
	0x88	INT Vector[95: 64]			
	0x8c	INT Vector[127: 96]			
	0x90	INT Vector[159: 128]			
	0x94	INT Vector[191: 160]			



	0x98	I NT Vector [223: 192]			
	0x9C	I NT Vector [255: 224]			
	0xA0	I NT Enabl e[31: 0]			
	0xA4	I NT Enabl e[63: 32]			
	0xA8	I NT Enabl e[95: 64]			
	0xAC	I NT Enabl e[127: 96]			
	0xB0	I NT Enabl e[159: 128]			
	0xB4	I NT Enabl e[191: 160]			
	0xB8	I NT Enabl e[223: 192]			
	0xBC	I NT Enabl e[255: 224]			
CAP 5 Gen3	0xC0	Capabi lity Type	Cap Enum/Index	Capabi lity Poi nter	Capabi lity ID
	0xC4	Gl obal Li nk Trai ni ng			
	0xC8	Transmi tter Confi gurati on 0			
	0xCC	Recei ver Confi gurati on 0			
	0xD0	Li nk Trai ni ng 0			
	0xD4	Frequency Extensi on			
	0xD8	Transmi tter Confi gurati on 1			
	0xDC	Recei ver Confi gurati on 1			
	0xE0	Li nk Trai ni ng 1			
	0xE4	BI ST Control			

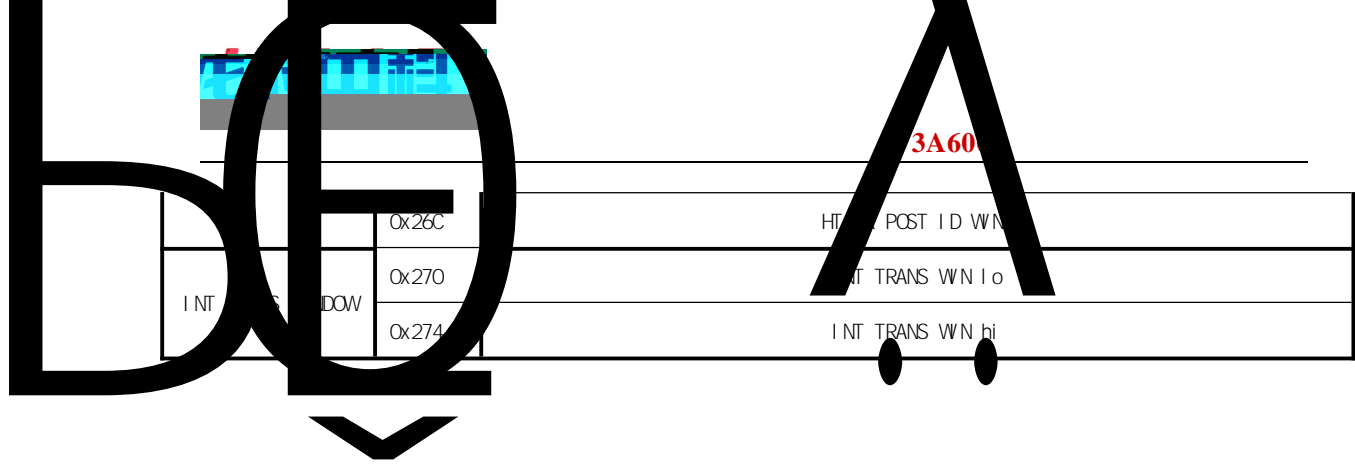
Enabl e	0x100	Devi ce ID		Vendor ID	
	0x104	Status		Command	
	0x108	Cl ass Code			Revi si on ID
	0x10c	BI ST	Header Type	Latency Ti mer	Cache Li ne Si ze
	0x110				
	0x114				
	0x118				
	0x11c				
	0x120				
	0x124				
	0x128	Cardbus Cl S Poi nter			



	0x12c	Subsystem ID	Subsystem Vendor ID
	0x130	Expansion ROM Enable Address	
	0x134	Reserved	Capabilities Pointer
	0x138	Reserved	
	0x13c	Bridge Control	Interrupt Pin
Receive Windows	0x140	HT RX Enable 0	
	0x144	HT RX Mask 0	
	0x148	HT RX Enable 1	
	0x14C	HT RX Mask 1	
	0x150	HT RX Enable 2	
	0x154	HT RX Mask 2	
	0x158	HT RX Enable 3	
	0x15C	HT RX Mask 3	
	0x160	HT RX Enable 4	
	0x164	HT RX Mask 4	
Header Trans	0x168	HT RX Header Trans	
	0x16C	HT RX EXT Header Trans	
Post Windows	0x170	HT TX Post Enable 0	
	0x174	HT TX Post Mask 0	
	0x178	HT TX Post Enable 1	
	0x17C	HT TX Post Mask 1	
Prefetchable Windows	0x180	HT TX Prefetchable Enable 0	
	0x184	HT TX Prefetchable Mask 0	
	0x188	HT TX Prefetchable Enable 1	
	0x18C	HT TX Prefetchable Mask 1	
Uncache Windows	0x190	HT RX Uncache Enable 0	
	0x194	HT RX Uncache Mask 0	
	0x198	HT RX Uncache Enable 1	
	0x19C	HT RX Uncache Mask 1	
	0x1A0	HT RX Uncache Enable 2	
	0x1A4	HT RX Uncache Mask 2	
	0x1A8	HT RX Uncache Enable 3	



	0x1AC	HT RX Uncache Mask	3
	0x1B0	HT RX P2P Enable	0
P2P	0x1B4	HT RX P2P Mask	0
Windows	0x1B8	HT RX P2P Enable	1
	0x1BC	HT RX P2P Mask	1
	0x1C0	APP Configuration	0
APP	0x1C4	APP Configuration	1
Config	0x1C8	RX Bus Value	
	0x1CC	PHY status	
	0x1D0	TX Buffer	0
Buffer	0x1D4	TX	



14.5.1 Bridge Control

0x3C
 0x00000000
 Bus Reset Control

14- 8 Bus Reset Control

31: 23	Reserved	9	0x0		
22	Reset	1	0x0	R/W	0- >1 HT_RSTn 0 1- >0 HT_RSTn 1
21: 0	Reserved	22	0x0		

14.5.2 Capability Registers

0x40
 0x00006008
 Command Capabilities Pointer Capability ID



	Pointer				
7:0	Capability ID	8	0x08	R	HyperTransport capability ID

0x44

0x00112000

Link Config Link Control

14- 10 Link Config Link Control



30:28	Link Width Out	3	0x0	R/W	HT Disconnect	000 8	001 16
27	Reserved	1	0x0				
26:24	Link Width In	3	0x0	R/W	HT Disconnect		
23	DwFc out	1	0x0	R			
22:20	Max Link Width out	3	0x1	R	HT		16bits
19	DwFc In	1	0x0	R			
18:16	u00 Ê						



3A6000

7:0

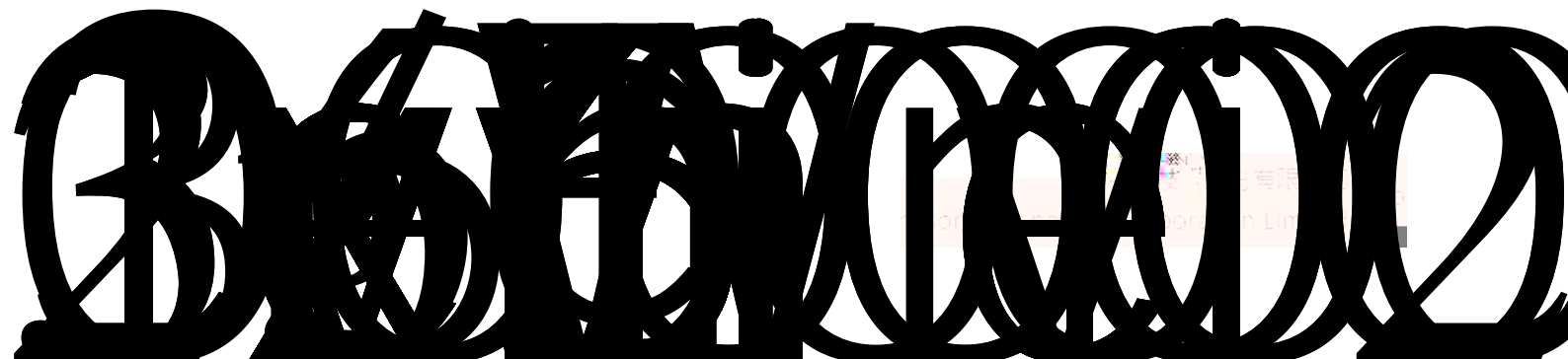
Revision ID

8

0x60

R/W

3:0



3A6000

3A6000



- [0, 4, 8, 12 252] 0
- [1, 5, 9, 13 253] 1
- [2, 6, 10, 14 254] 2
- [3, 7, 11, 15 255] 3

ht_int_stripe_1

0x80

0x00000000

HT [31: 0]

14- 20 HT 1

31: 0	Interrupt_case [31: 0]	32	0x0	R/W	HT [31: 0]

0x84

0x00000000

HT [63: 32]

14- 21 HT 2

31: 0	Interrupt_case [63: 32]	32	0x0	R/W	HT [63: 32]

0x88

0x00000000

HT [95: 64]

14- 22 HT 3

31: 0	Interrupt_case [95: 64]	32	0x0	R/W	HT [95: 64]

0x8c

0x00000000

HT [127: 96]

14- 23 HT 4

--	--



14.5.8

256

1

0

256

14.5.7

0xa0

0x00000000

HT

[31:0]

14- 27 HT

1



31:0 Interrupt_mask
[31:0]

32 0x0 R/W H1 H



14- 30 HT

4

31: 0	Interrupt_mask [127: 96]	32	0x0	R/W	HT	[127: 96]

0xb0

0x00000000

HT [159: 128]

14- 31 HT

5

31: 0	Interrupt_mask [159: 128]	32	0x0	R/W	HT	[159: 128]

0xb4

0x00000000

HT [191: 160]

14- 32 HT

6

31: 0	Interrupt_mask [191: 160]	32	0x0	R/W	HT	e [191: 160]



14.5.10

HT

hit = (BASE & MASK) == (ADDR & MASK)

addr_out_trans addr



3A6000

15: 0	ht_rx_image0_mask[39: 24]	16	0x0	R/W	HT	0	[39: 24]
-------	----------------------------	----	-----	-----	----	---	-----------

0x148

0x00000000

HT 1

14- 38 HT 1



31	ht_rx_image1_en	1	0x0	R/W	HT	1
30	ht_rx_image1_trans_en	1	0x0	R/W	HT	1
29	ht_rx_image1_multi_node_en	1	0x0	R/W	HT	1

[39: 37]



						[39: 37] [46: 44]
28	ht_rx_image2_conf_hi_t_en	1	0x0	R/W	HT	2
0						
25: 0	ht_rx_image2_trans[49: 24]	26	0x0	R/W	HT	2 [49: 24]

0x154

0x00000000

HT 2

14- 41 HT 2

31: 16	ht_rx_image2_base[39: 24]	16	0x0	R/W	HT	2 [39: 24]
15: 0	ht_rx_image2_mask[39: 24]	16	0x0	R/W	HT	2 [39: 24]

0x158

0x00000000

HT 3

14- 42 HT 3

|--|--|--|--|--|--|--|

31 ht_rx_image3_en 1 0x0 R/W HT 3

30 ht_rx_image3_trans_en 1 -



Bit Range	Field Name	Width	Reset Value	Access	HT	Count	Range
31: 16	ht_rx_image3_base[39: 24]	16	0x0	R/W	HT	3	[39: 24]
15: 0	ht_rx_image3_mask[39: 24]	16	0x0	R/W	HT	3	[39: 24]

0x160

0x00000000

HT 4

14- 44 HT 4

Bit Range	Field Name	Width	Reset Value	Access	HT	Count	Range
31	ht_rx_image4_en	1	0x0	R/W	HT	4	
30	ht_rx_image4_trans_en	1	0x0	R/W	HT	4	
29	ht_rx_image4_multi_node_en	1	0x0	R/W	HT	4	[39: 37] [46: 44]
28	ht_rx_image4_conf_hit_en	1	0x0	R/W	HT	4	0
25: 0	ht_rx_image4_trans[49: 24]	26	0x0	R/W	HT	4	[49: 24]

0x164

0x00000000

HT 4

14- 45 HT 4

Bit Range	Field Name	Width	Reset Value	Access	HT	Count	Range
31: 16	ht_rx_image4_base[39: 24]	16	0x0	R/W	HT	4	[39: 24]
15: 0	ht_rx_image4_mask[39: 24]	16	0x0	R/W	HT	4	[39: 24]

14.5.11

HT

0x168

0x00000000

14- 46



3A6000



0xFD_FE000000

31	ht_rx_header_trans_ext	1	0x1	R/W	type1	24	28
----	------------------------	---	-----	-----	-------	----	----

EXT HEADER

30	ht_rx_header_trans_en						
----	-----------------------	--	--	--	--	--	--



3A6000



ACC)

29.23 V



0x00000000

HT POST 2

14- 52 HT POST 2

Bit Range	Field Name	Width	Default	Access	Attributes	Cache	Other
31	ht_post2_en	1	0x0	R/W	HT POST	2	
30	ht_split2_en	1	0x0	R/W	HT (ACC)	CPU uncache	
29: 23	Reserved	14	0x0				
15: 0	ht_post2_trans[39: 24]	16	0x0	R/W	HT POST	2	[39: 24]

0x3A4

0x00000000

HT POST 2

14- 53 HT POST 2

31: 16	ht_post2_base[39: 24]	16	0x0	R/W	HT POST	2	[39: 24]
15: 0	ht_post2_mask[39: 24]	16	0x0	R/W	HT POST	2	[39: 24]

0x3A8

0x00000000

HT POST 3

14- 54 HT POST 3

31	ht_post3_en	1	0x0	R/W	HT POST	3	
30	ht_split3_en	1	0x0	R/W	HT (ACC)	CPU uncache	
29: 16	Reserved	14	0x0				
15: 0	ht_post3_trans[39: 24]	16	0x0	R/W	HT POST	3	[39: 24]

0x3Ac

0x00000000

HT POST 3



14- 55 HT POST 3

31: 16	ht_post3_base[39: 24]	16	0x0	R/W	HT	POST	3	[39: 24]
15: 0	ht_post3_mask[39: 24]	16	0x0	R/W	HT	POST	3	[39: 24]

14.5.13

14.5.10

HT AXI CACHE HT CACHE

0x180
0x00000000
HT 0

14- 56 HT 0

31	ht_prefetch0_en	1	0x0	R/W	HT	0	
30: 16	Reserved	15	0x0				
15: 0	ht_prefetch0_trans[39: 24]	16	0x0	R/W	HT	0	[39: 24]

0x184
0x00000000
HT 00 2 = ê

14- 57 HT 0



3A6000

14- 58 HT

1



31 ht_prefetch1_en 1 0x0 R/W HT etch



3A6000



28	ht_uncache0_conf_hit_en	1	0x0	R/W	HT	uncache	0
25: 0	ht_uncache0_trans[49: 24]	26	0x0	R/W	HT	uncache	0



3A6000

14- 63 HT

Uncache

1



31: 16



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31	ht_uncache3_en	1	0x0	R/W	HT	uncache	3
30	ht_uncache3_trans_en	1	0x0	R/W	HT		

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					0 -> 1		
					LDT_DISCONNECT	HT	
					LDT_REQ_n		
28	Ldt Req Gen	1	0x0	R/W	0	1	0 -> 1
27	rx sample en	1	0x0	R/W	cad	ctl	0x1c8
26	Dword Write	1	0x1	R/W	32/64/128/256	MEM	

3A6000

3A6000

15	Crc Interrupt	1	0x0	R/W	CRC	111 0	
14:12	Crc Interrupt route	3	0x0	R/W	CRC		
11	Reserved						
10	ht interrupt 8 bit	1	0x0	R/W	8	3	
9:8	ht_interrupt_stripe	2	0x0	R/W	0x0 ht_interrupt_stripe_1 0x1 ht_interrupt_stripe_2 0x2 ht_interrupt_stripe_4		
							SMI NMI INT
							INTTH
4:0	Interrupt Index	5	0x0	R/W			

14.5.18 PHY

PHY

0x1CCC

0x83308000

PHY

14- 75 PHY

Bit Range	Field Name	Width	Reset Value	Access	Field Name	Width
31: 29	Reserved	3	0x0	R		
28	dll Locked hi	1	0x0	R	8 DLL	
27	dll Locked lo	1	0x0	R	8 PLL	
26	cdr Locked hi	1	0x0	R	8 CDR	
25	cdr Locked lo	1	0x0	R	8 CDR	
24	phase Locked	1	0x0	R		
23: 20	phy state	4				



14- 76



31: 24	B_CMD_txbuffer	8	0x0	R	B
23: 16	R_CMD_txbuffer	8	0x0	R	R
15: 8	NPC_CMD_txbuffer	8	0x0	R	NPC, p



3A6000

7:0	PC_DATA_txbuffer	8	0x0	R	PC
-----	------------------	---	-----	---	----

14.5.21

HT

0x1D8

0x00000000

14- 78





7: 4 NPC_CMD_txadj 4 0x0 R/W



14- 83 Training 2

			= }		
31: 0	T2 time	32	0x7fffff	R/W	Training 2

14.5.27 Training 3

HyperTransport 3.0 Training 3

HyperTransport 3.0 1/4

0x1F0

Training 3

14- 84 Training 3

--	--	--	--	--	--

31: 0 T3 time 32



HyperTransport 3.0:

PHY_LINK_CLK 100MHz × div_loop /div_refc /phy_div
PLL systemclk 33M 30us

3C5000 HT_CORE_CLK NODE

0x1F4

0x00000000

14- 85

31	Reserved	1	0x0	R/W	
30-26	Soft_phy_hi_div	5	0x0	R/W	PHY
25	Reserved	1	0x0	R/W	
24-20	Soft_phy_lo_div	5	0x0	R/W	PHY
19-17	Reserved	3	0x0	R/W	
16-8	Soft_div_loop	9	0x0	R/W	PLL
7-4	Soft_div_refc	4	0x0	R/W	PLL
3	Locked	1	0x0	R	
2	Bypass ht core	1	0x0	R/W	
1	Soft_config_enable	1	0x0	R/W	1' b0 1' b1
0	Reserved	1	0x0	R/W	

14.5.29 PHY

PHY

0x1F8

0x00000000

PHY

14- 86

--	--	--	--	--	--



31	Tx_scani_n_en	1	0x0	R/W	TX
30	Rx_scani_n_en	1	0x0	R/W	RX
27: 24	Tx_scani_n_ncode	4	0x0	R/W	TX ncode
23: 20	Tx_scani_n_pcode	4	0x0	R/W	TX pcode
19: 12	Rx_scani_n_code	8	0x0	R/W	RX

14.5.30 PHY

PHY 8bi t
 PHY PHY 1 16bi t
 PHY
 0x1FC
 0x83308000
 PHY

14- 87 PHY

31	Rx_ckpll_term	1	0x1	R/W	PLL RX
30	Tx_ckpll_term	1	0x0	R/W	PLL TX
29	Rx_clk_i_n_sel	1	0x0	R/W	PAD PAD HT1 CLKPAD 1' b0 1' b1 PLL
28	Rx_ckdll_sel	1	0x0	R/W	DLL 1' b0 PLL 1' b1
27: 26	Rx_ctl_e_b1tc	2	0x0	R/W	PAD EQD
25: 24	Rx_ctl_e_b1tr	2	0x3	R/W	PAD EQD
23: 22	Rx_ctl_e_b1tlm	2	0x0	R/W	PAD EQD
21	Rx_en_lldo	1	0x1	R/W	LDO 1' b0 LDO 1' b1 LDO



31: 16	Rx_wait_time	16	0x0	R/W	RX
15: 0	Tx_wait_time	16	0x0	R/W	TX

0x248

0x00000000

LDT 2

14- 90 LDT 2

31: 30	Reserved	16	0x0	R/W	
29: 0	rx_lane_ts_0	16	0x0	R/W	

0x24C

0x00000000

LDT 3

14- 91 LDT 3

31: 30	Reserved	16	0x0	R/W	
29: 0	rx_lane_ts_1	16	0x0	R/W	

0x250

0x00000000

LDT 4

14- 92 LDT 4

31: 30	Reserved	16	0x0	R/W	
29: 0	rx_lane_ts_2	16	0x0	R/W	

0x254

0x00000000

LDT 5



14- 93 LDT

5



31: 22	Reserved	10	0x0	R/W
21: 18	wait ctl	4	0x0	R/W
17: 0	phase lock	18	0x0	I



					I D MASK
15: 0	HT TX POST I D1 BASE	16	0x0	R/W	AXI I D POST I D BASE

0x268
0x00000000
HT TX POST I D WN2

14- 97 HT TX POST ID WIN2

31: 16	HT TX POST I D2 MASK	16	0x0	R/W	AXI I D POST I D MASK
15: 0	HT TX POST I D2 BASE	16	0x0	R/W	AXI I D POST I D BASE

0x26C
0x00000000
HT TX POST I D WN3

14- 98 HT TX POST ID WIN3

31: 16	HT TX POST I D3 MASK	16	0x0	R/W	AXI I D POST I D MASK
15: 0	HT TX POST I D3 BASE	16	0x0	R/W	AXI I D POST I D BASE



14.5.36 Bist

HT bist
 0x340
 0x00000010
 bist

14- 102 bist

31: 5	Reserved	27	0x0	R/W	
4	bist_resetn	1	0x1	R/W	bist
3	bist_fail	1	0x0	R/W	bist
2	prbs_lpbk_en	1	0x0	R/W	prbs
1	prbs_32	1	0x0	R/W	prbs_32
0	bist_mode	1	0x0	R/W	bist

0x344
 0x00000000
 bist 0

14- 103 bist 0

31: 8	bist_error_bit0	24	0x0	R/W	bist
7: 0	bist_error_cnt0	8	0x0	R/W	bist bit

0x348
 0x00000000
 bist 1

14- 104 bist 1

31: 8	bist_error_bit1	24	0x0	R/W	bist
7: 0	bist_error_cnt1	8	0x0	R/W	bist bit



14.5.37 LDO

PHY LDO
0x350
0xBFA38783
LDO

14- 105 LDO





14.5.40 Unitid

id HT unitid
 0x360
 0x00000000
 unitid 0
 14- 108 unitid 0

31: 21	Reserved	11	0x0	R/W	
23: 16	unit_id0	5	0x0	R/W	0 unitid
15: 8	axi2unitid0_mask	8	0x0	R/W	0 id
7: 0	axi2unitid0_base	8	0x0	R/W	0 id



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7: 0	axi 2uni ti d2_base	8	0x0	R/W	2	i d
------	---------------------	---	-----	-----	---	-----

0x36C

0x00000000

uni ti d 3

14- 111 unitid 3



31: 21	Reserved	11	0x0	R/W		
23: 16	uni t_j d3	5	0x0	R/W	3	uni ti d
15: 8	axi 2uni ti d3_mask	8	0x0	R/W	3	i d
7: 0	axi 2uni ti d3_base	8	0x0	R/W	3 d	" "

↓

BS

Dz



19: 15	LC_VTH1_CTRL_N	5	0x18	R/W	
14: 10	LC_VTH1_CTRL_P	5	0x18	R/W	
9: 5	LC_VTH2_CTRL_N	5	0x18	R/W	
4: 0	LC_VTH2_CTRL_P	5	0x18	R/W	

14.5.44 PLL

PLL

0x37C

0x0000600F

PLL

14- 115 PLL





HT

POST

NONPOST

0x1C0[17: 16]

0 3

0x380

0x00000000

HT 0

14- 116 HT 0

31	ht_rx_prior0_en	1	0x0	R/W	HT	0
30	ht_rx_prior0_post_en	1	0x0	R/W	HT	0 POST
29	ht_rx_prior0_nonpost_en	1	0x0	R/W	HT	0 NONPOST
1: 0	ht_rx_prior0	2	0x0	R/W	HT	0

0x384

0x00000000

HT 0

14- 117 HT 0

31: 16	ht_rx_prior0_base[39: 24]	16	0x0	R/W	HT	0 [39: 24]
15: 0	ht_rx_prior0_mask[39: 24]	16	0x0	R/W	HT	0 [39: 24]

0x1B8

0x00000000

HT 1

14- 118 HT 1

31	ht_rx_prior1_en	1	0x0	R/W	HT	1
30	ht_rx_prior1_post_en	1	0x0	R/W	HT	1 POST
29	ht_rx_prior1_nonpost_en	1	0x0	R/W	HT	1 NONPOST
1: 0	ht_rx_prior1	2	0x0	R/W	HT	1



0x1BC
0x00000000
HT 1

14- 119 HT 1

31: 16	ht_rx_pri or 1_base[39: 24]	16	0x0	R/W	HT	1	[39: 24]
15: 0	ht_rx_pri or 1_mask[39: 24]	16	0x0	R/W	HT	1	[39: 24]

14.5.46

14. 5. 10

HT 0xFD_0xxx_xxxx

0x3C0
0x00000000
HT 0

14- 120 HT 0

31	ht_rx_i r0_en	1	0x0	R/W	HT	0	
----	---------------	---	-----	-----	----	---	--

0x3C4
0x00000000
HT 0

14- 121 HT 0

31: 16	ht_rx_i r0_base[39: 24]	16	0x0	R/W	HT		[39: 24]
15: 0	ht_rx_i r0_mask[39: 24]	16	0x0	R/W	HT		[39: 24]

14.6 HyperTransport

HyperTransport PCI

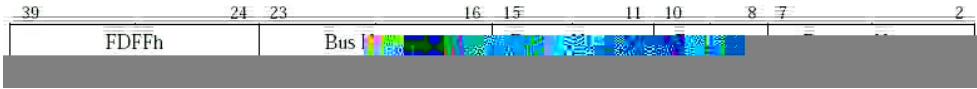


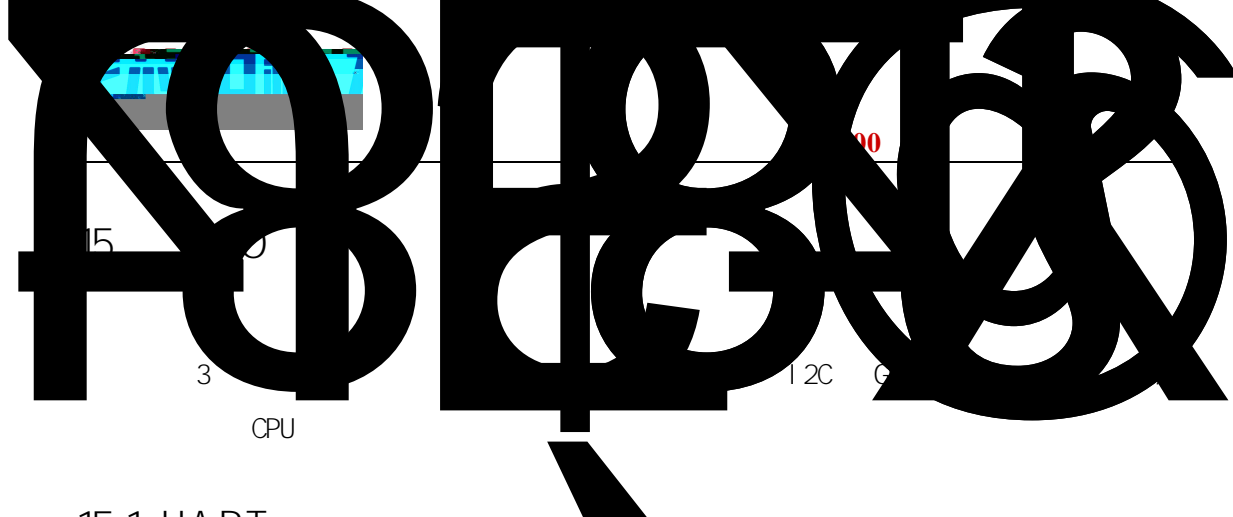
		36- 8	HT	
0xFD_FE00_0000	0xFD_FFFF_FFFF	HT		3A6000

Type 0:

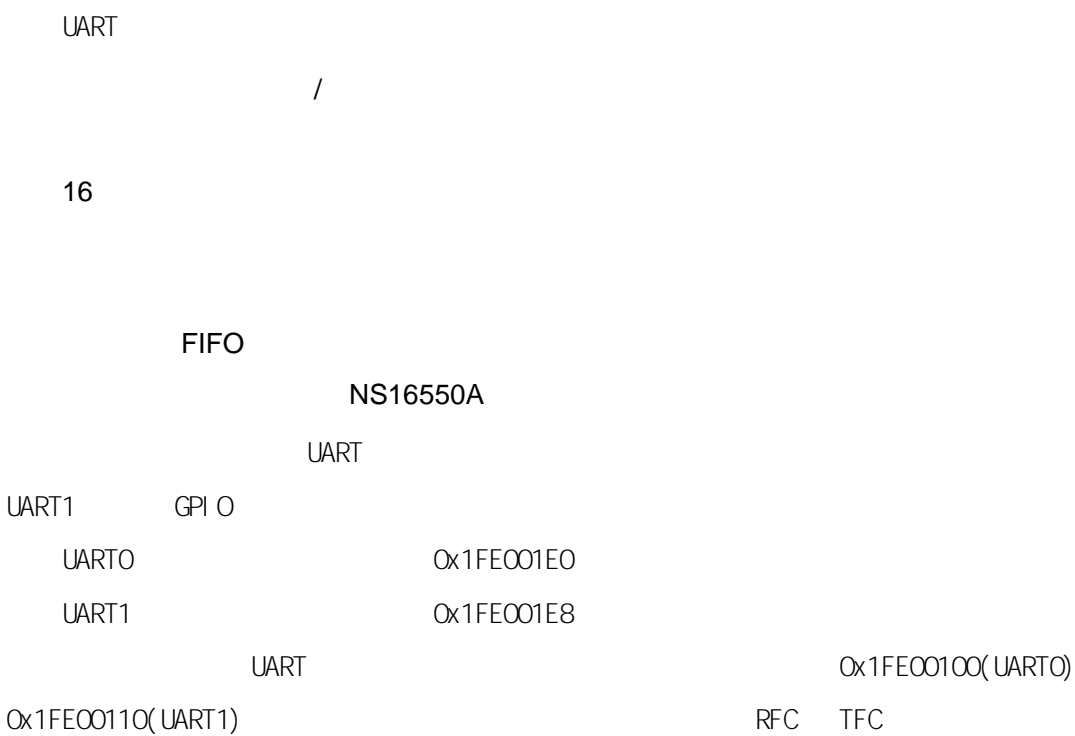


Type 1:





15.1 UART



15.1.1 DA q q



15.1.2 IER

[7 0]
0x01
0x00

Bit	Field	Width	Access	Description
7:4	Reserved	4	RW	
3	IME	1	RW	Modem '0' - '1' -
2	ILE	1	RW	'0' - '1' -
1	ITxE	1	RW	'0' - '1' -
0	IRxE	1	RW	'0' - '1' -

15.1.3 IIR

[7 0]
0x02
0xc1

Bit	Field	Width	Access	Description
7:4	Reserved	4	R	
3:1	II	3	R	
0	INTp	1	R	

Bit 3	Bit 2	Bit 1	Field	Description
0	1	1	1st	LSR
0	1	0	2nd	FIFO trigger FIFO trigger



3A6000

1	1	0	2nd		FIFO	FIFO
					4	
0	0	1	3rd			THR
						IIR
0	0	0	4th	Modem		



				' 0' -
5	spb	1	RW	' 0' - ' 1' - LCR[4] 1 0 LCR[4] 0 1
4	eps	1	RW	' 0' - 1 ' 1' - 1
3	pe	1	RW	' 0' - ' 1' -
2	sb	1	RW	' 0' - 1 ' 1' - 5 1.5 2
1: 0	bec	2	RW	' 00' - 5 ' 01' - 6 ' 10' - 7 ' 11' - 8

15.1.6 MODEM

MCR

Modem

[7 0]

0x04

0x00



7: 5	Reserved	3	W
4	Loop	1	W

' 0' -
' 1' -



				DTR : DSR RTS : CTS Out1 : RI Out2 : DCD
3	OUT2	1	W	DCD
2	OUT1	1	W	RI
1	RTSC	1	W	RTS
0	DTRC	1	W	DTR

15.1.7

LSR

[7 0]
0x05
0x00



7	ERROR	1	R	' 1' -
				' 0' -
6	TE	1	R	' 1' - FIFO



3	FE	1	R	' 1' - ' 0' -
2	PE	1	R	' 1' - ' 0' -
1	OE	1	R	' 1' - ' 0' -
0	DR	1	R	' 0' - FI FO ' 1' - FI FO

LSR[4: 1] LSR[7] LSR[6: 5] FI FO

LSR[0] FI FO

15.1.8 MODE8



15.1.9 FIFO RFC

FIFO

[7 0]

0x08

0x00



7:0

RFC

3

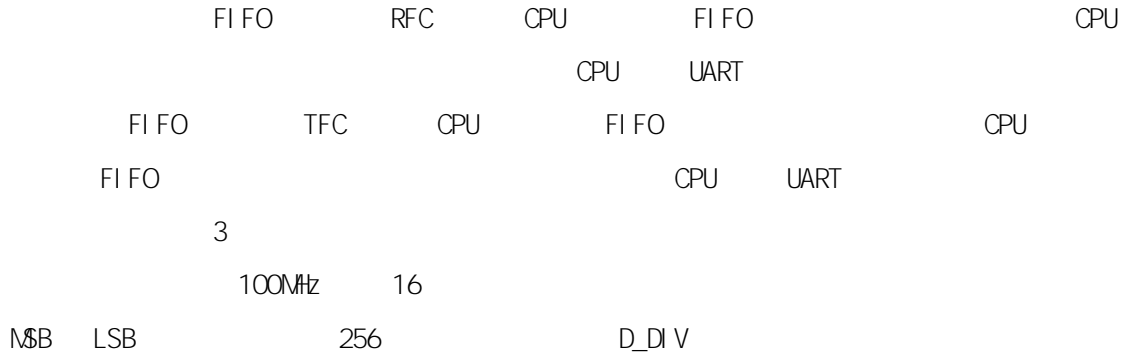


0x02

0x00

7: 0	D_DIV	8	RW	

15.1.12



15.2 SPI

SPI

4

SPI

SPI

Dual/Quad mode SPI flash

SPI

0x1FE001F0

15- 1 SPI

SPI Boot	0x1C00_0000- 0x1CFF_FFFF	16MByte
SPI Memory	0x1D00_0000- 0x1DFF_FFFF	16MByte
SPI Register	0x1FE0_01F0- 0x1FE0_01FF	16Byte



SPI Boot

SPI Memory

CPU

15.2.1

SPCR

[7 0]

0x00

0x10

Bit	Field	Width	Access	Value
7	Spi e	1	RW	
6	spe	1	RW	
5	Reserved	1	RW	
4	nsr	1	RW	master 1
3	cpol	1	RW	
2	cpha	1	RW	1 0
1:0	spr	2	RW	scl k_o sper spre

15.2.2

SPSR

[7 0]

0x01

0x05

Bit	Field	Width	Access	Value
7	spi f	1	RW	1 1
6	wcol	1	RW	1 , 1
5:4	Reserved	2	RW	
3	wffull	1	RW	1
2	wfempty	1	RW	1
1	rffull	1	RW	1
0	rfempty	1	RW	1



15.2.3 Tx FIFO

[7 0]
0x02
0x00

7:0	Tx FIFO	8	W	
-----	---------	---	---	--

15.2.4 SPER

[7 0]
0x03
0x00

7:6	i cnt	2	RW	00 - 1 01 - 2 10 - 3 11 - 3
5:2	Reser ved	4	RW	
1:0	spre	2	RW	Spr

spre	00	00	00	00	01	01	01	01	10	10	10	10
spr	00	01	10	11	00	01	10	11	00	01	10	11
	2	4	16	32	8	64	128	256	512	1024	2048	4096

15.2.5 SFC_PARAM

SPI Flash
[7 0]
0x04
0x21



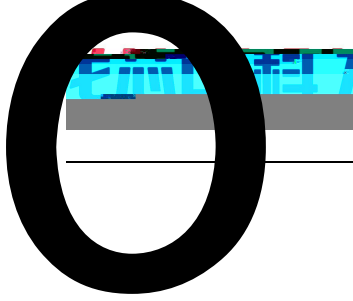
7:4	cl k_di v	4	RW	{spre, spr}
3	dual_i o	1	RW	I/O
2	fast_read	1	RW	
1	burst_en	1	RW	spi fl ash
0	memory_en	1	RW	spi fl ash csn[0]

15.2.6

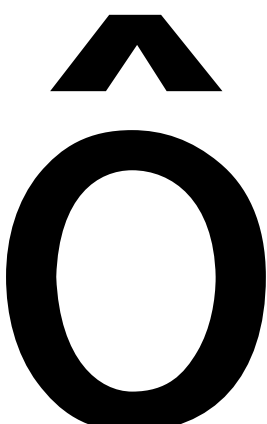
SFC_SOFTCS

SPI Flash

S> C



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15.2.11

1 BUF1

SPI Flash

1

[7 0]

0x0b

0x00



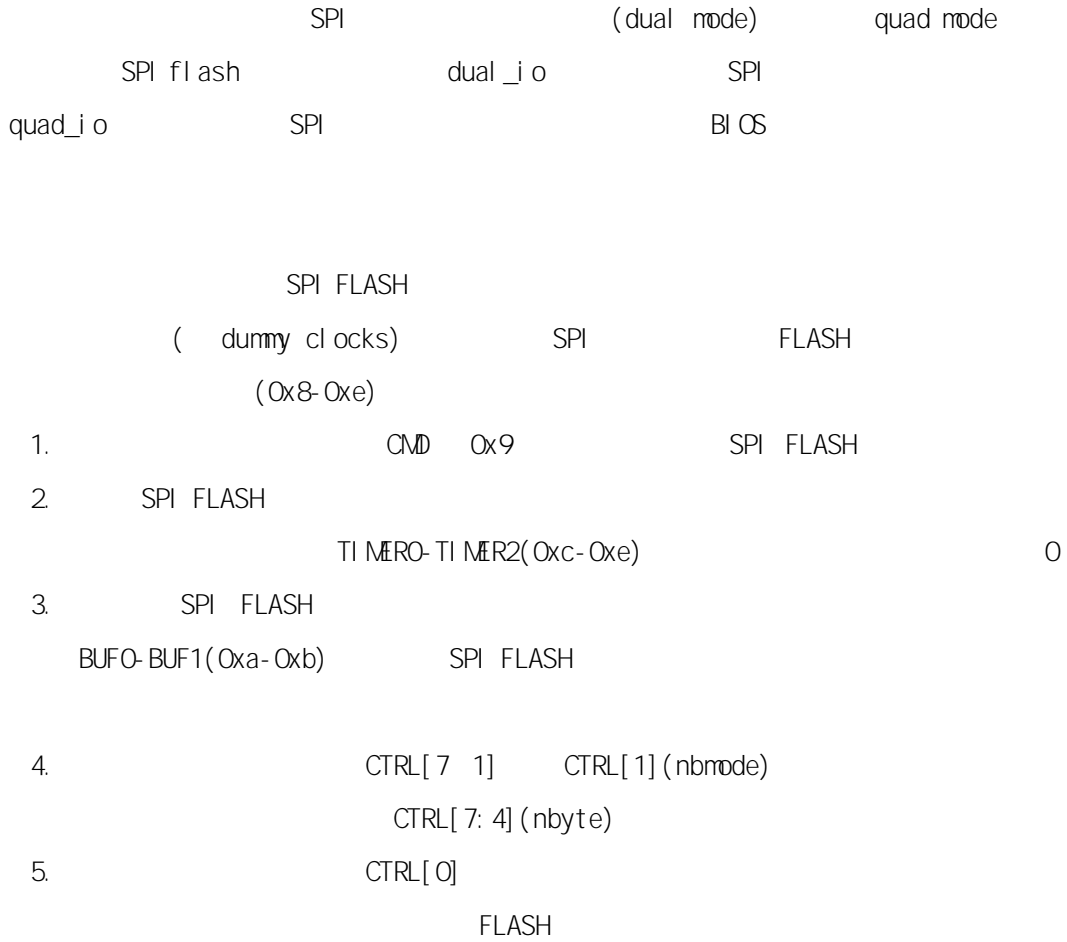


0x0e

0x00

7:0	time2	8	RW	8
-----	-------	---	----	---

15.2.15 SPI



15.3 I2C





SLV_CTRL[6:0]

I 2C0 0x1FE00120

I 2C1 0x1FE00130

15.3.1 PRERlo

[7:0]

0x00

0xff

7:0	PRERlo	8	RW	

15.3.2 PRERhi

[7:0]

0x01

0xff

7:0	PRERhi	8	RW	

prescale LPB PCLK clock_aSCL

clock_s

$$\text{Prescale} = \text{clock}_a / (4 * \text{clock}_s) - 1$$

15.3.3 CTR

[7:0]

0x02

0x20

--	--



7	EN	1	RW	1 0
6	IEN	1	RW	1
5	MST_EN	1	RW	0 slave 1 master
4:0	Reserved	5	RW	

15.3.4 TXR

[7 0]
0x03
0x00

7:1	DATA	7	W	
0	DRW	1	W	

15.3.5 RXR

[7 0]
0x03
0x00

7:0	RXR	8	R	

15.3.6 CR

[7 0]



0x04

0x00

7	STA	1	W	START
6	STO	1	W	STOP
5	RD	1	W	
4	WR	1	W	
3	ACK	1	W	
2:1	Reserved	2	W	
0	IACK	1	W	

I2C

bit 3 1

ack

ack

15.3.7

SR

[7:0]

0x04

0x00

7	RxACK	1	R	1 0
6	Busy	1	R	I2C 1 0
5	AL	1	R	I2C I2C 1
4:2	Reserved	3	R	
1	TIP	1	R	1 0
0	IF	1	R	1



15.3.8 SLV_CTRL

[7 0]

0x07

0x00

7	SLV_EN	1	WR	MST_EN 0
6 0	SLV_ADDR	7	WR	1 2C

15.4 AVS

AVS

0x1FE00160

15- 2 AVS

AVS Register	0x1FE0_0160-0x1FE0_016F	16B
--------------	-------------------------	-----

15.4.1 CSR

[31 0]

0x0

0x0

31	resyn	1	RW	1 0 0
30-29	mask_ack	2	RW	1 mask alert_ack
28	mask_i	1	RW	1 mask alert_i
27	mask_s	1	RW	1 mask alert_s
26	mask_c	1	RW	1 mask alert_c
25	mask_a	1	RW	1 mask alert_a
24	rx_ctrl	1	RW	1 AVS 0 AVS



				0
23: 20	rx_delay	4	RW	1 2 0
19: 17	clk_div	3	RW	0x0 0x1 0x2 0x3 0x4 0x5
16	Dmux	1	RW	1 0 0
15: 0	reserved	16	—	—

15.4.2 Mreg

[31 0]
0x4
0x0

31	TX_EN	1	RW	1	AVS
30: 29	cmd	2	RW	0x0	0x1 0x2 0x3 cmd
28	group	1	RW	0	AVS 1
27: 24	cmd_type	4	RW	0x0	1LSB=1mV 0x1 cmd_data 0x2 0x3 0x4 0x5 0x6-0xd 0xe 0xf
23: 20	rail_sel	4	RW		0xf
19: 4	cmd_data	16	RW		
3: 0	reserved			0	1

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